ELECTROHOME
Projection Systems

Control Module Specification
00-150306-01P

Assembly: 02-260306-04P
Schematic: 00-270306-02P

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Revision History

Iss.	Date	ECN	Page	Change	Approval
01	08/20/93			Original	A.K.

1.0 Functional Description

The Control Module (CLM) is contained in the rear card cage of the Marquee projector. It provides embedded software, timing signals and many waveforms essential to the projector's operation. The module consists nominally of two boards: the Control Board and the Deflection Processor Board (DPB). The DPB is a daughterboard which is attached to the larger Control Board. An second daughterboard, the Stigmator Waveform Board (SWB), can also be installed. It is included on the Control Module in the Marquee 9000 projector.

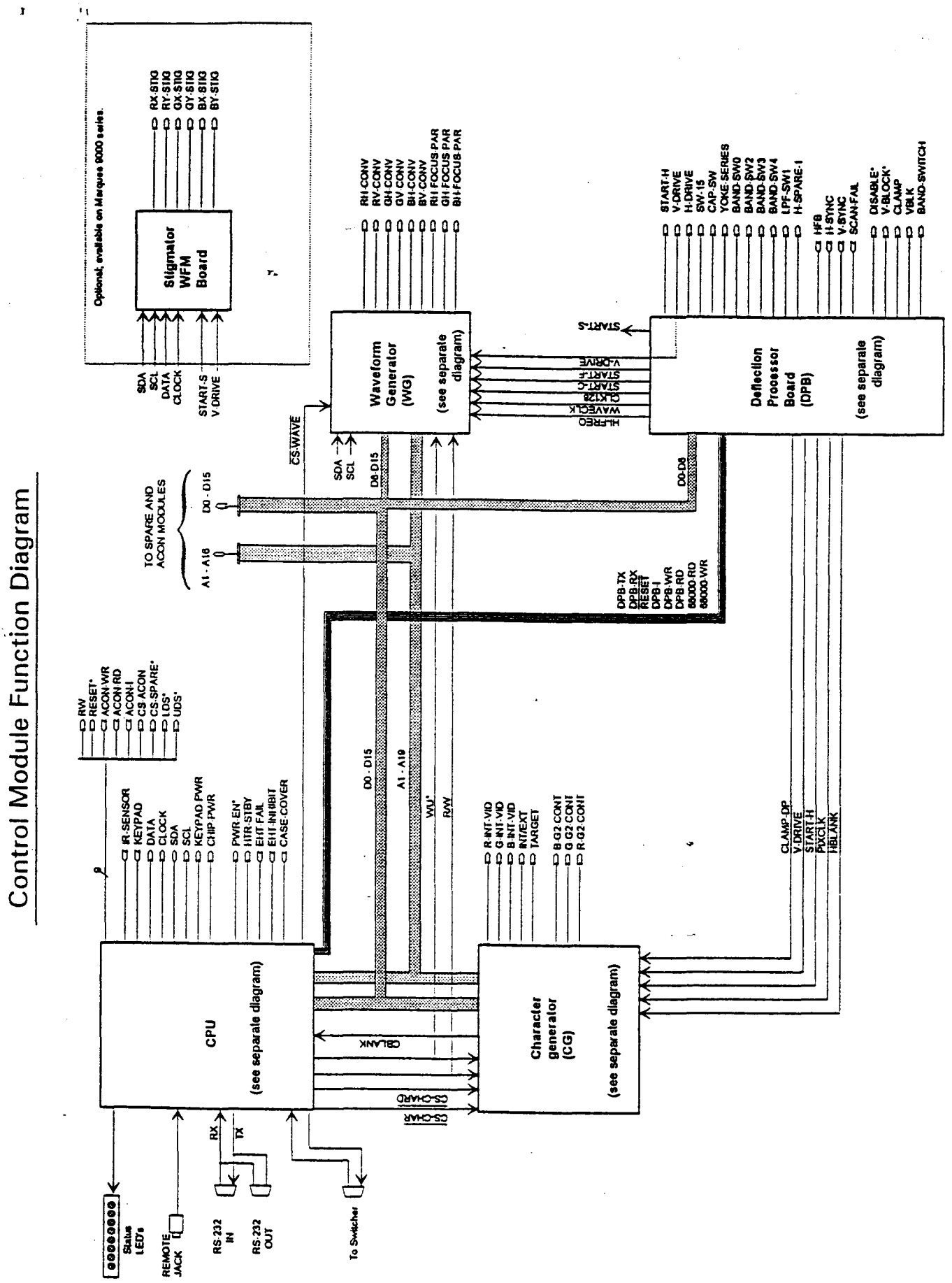
The Control Board is functionally divided into three sections; the CPU, the Waveform Generator and the Character Generator. The CPU runs the system software and controls the other modules in the projector. It accepts user input from hand-held keypads and communicates with devices external to the projector using RS-232. The Waveform Generator creates convergence waveforms for the Convergence Amplifier (CVA) and horizontal rate dynamic focus waveforms for the Focus Module (FCM). The Character Generator outputs analog RGB video signals to the Video Input Module (VIM) for displaying on-screen menus and test patterns. It also outputs G2 control voltages to the High Voltage Power Supply (HVPS).

The DPB generates horizontal and vertical drive signals for the Horizontal Deflection Module (HDM) and Vertical Deflection Module (VDM), respectively. Additionally, it outputs numerous control signals to the HDM and FCM to define frequency bands and to control switching between those bands. The DPB also generates clocks and other timing signals for the Waveform Generator and the Character Generator.

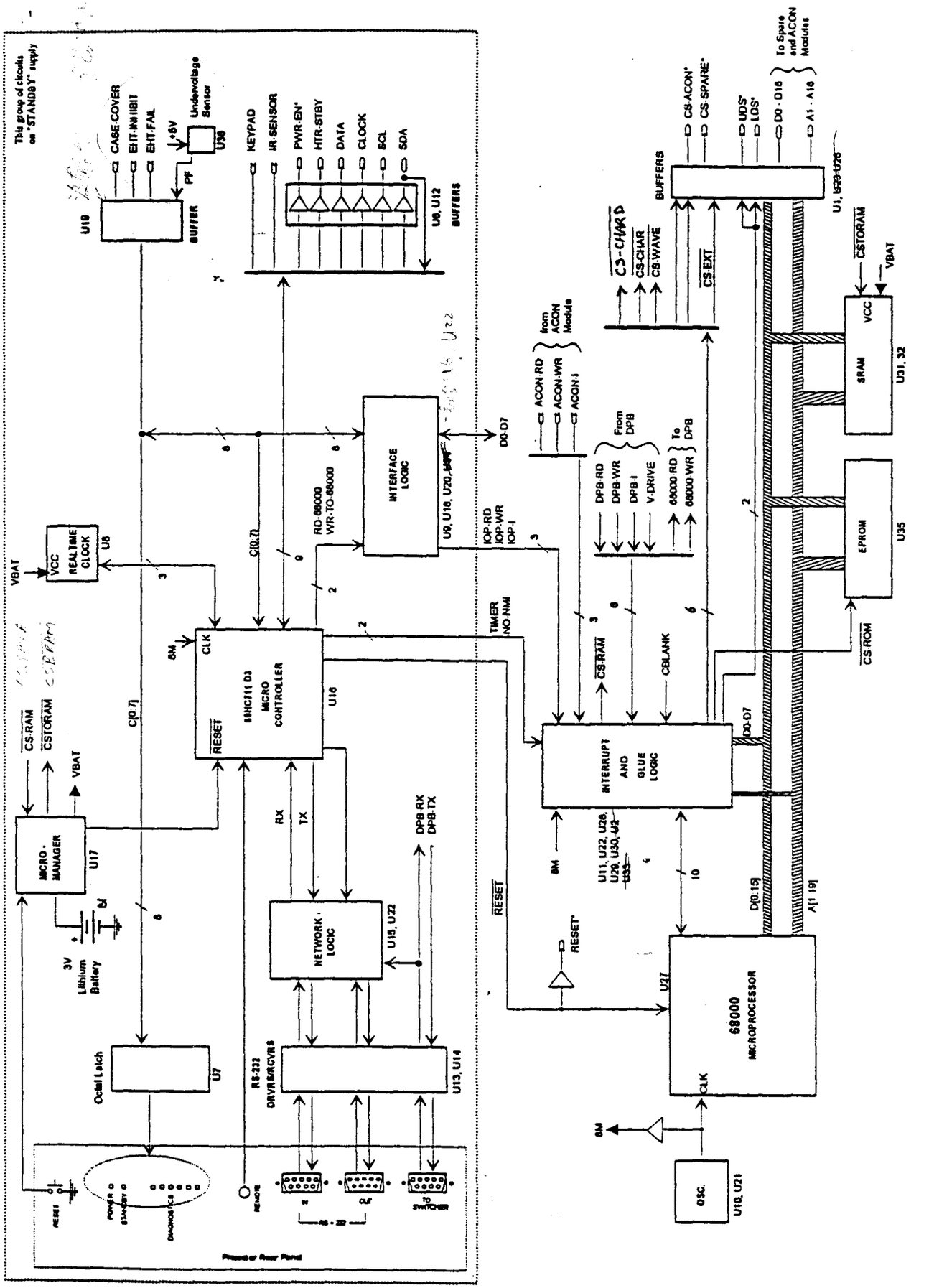
Four block diagrams are included in this section. The first illustrates the major sections of the Control module and the signals that connect them together. The remaining three diagrams shows in block form the internal details of the CPU, Waveform Generator and Character Generator.

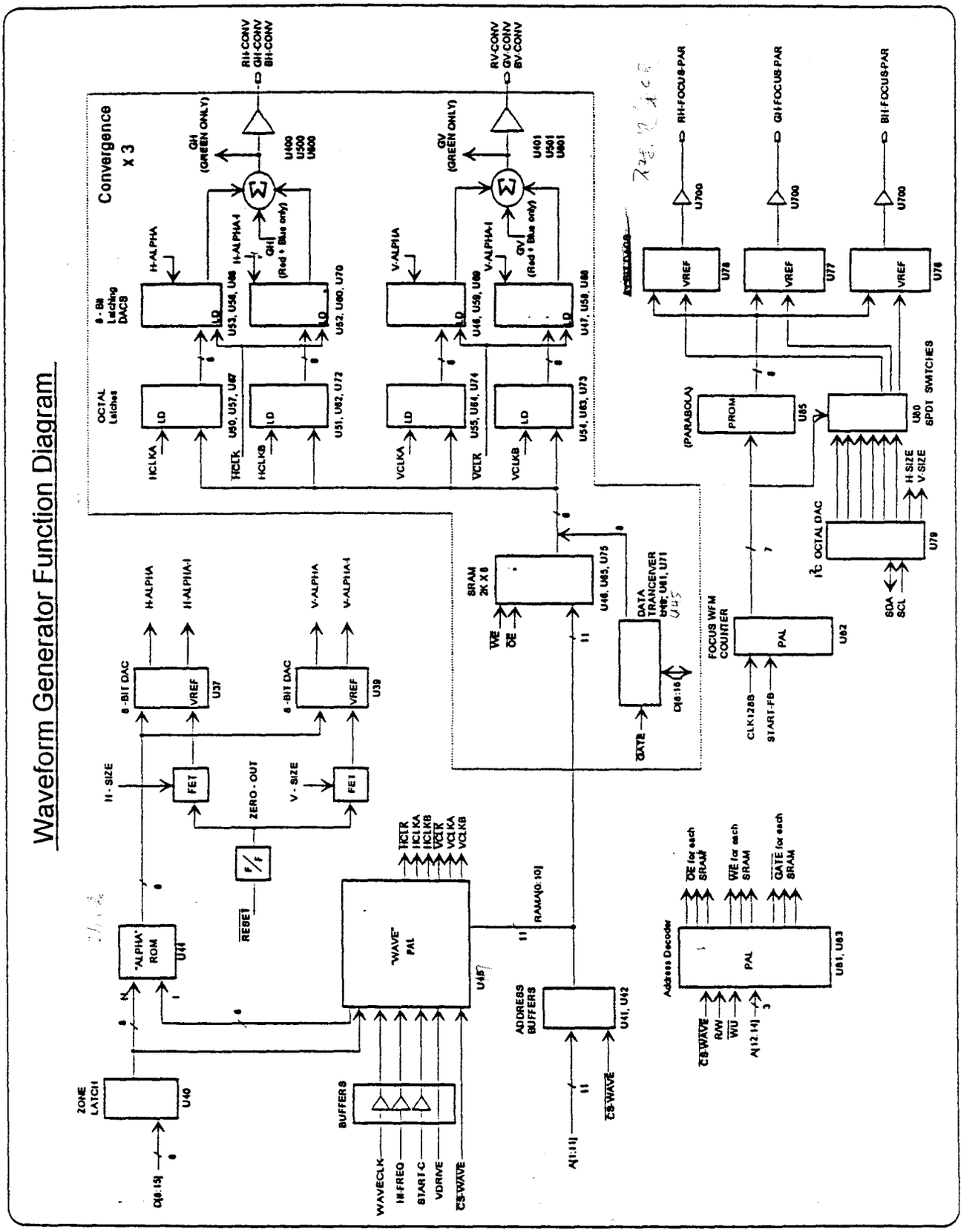
This document describes only the main Control Board. The DPB is fully described in specification document 00-151306-01P.

Control Module Function Diagram

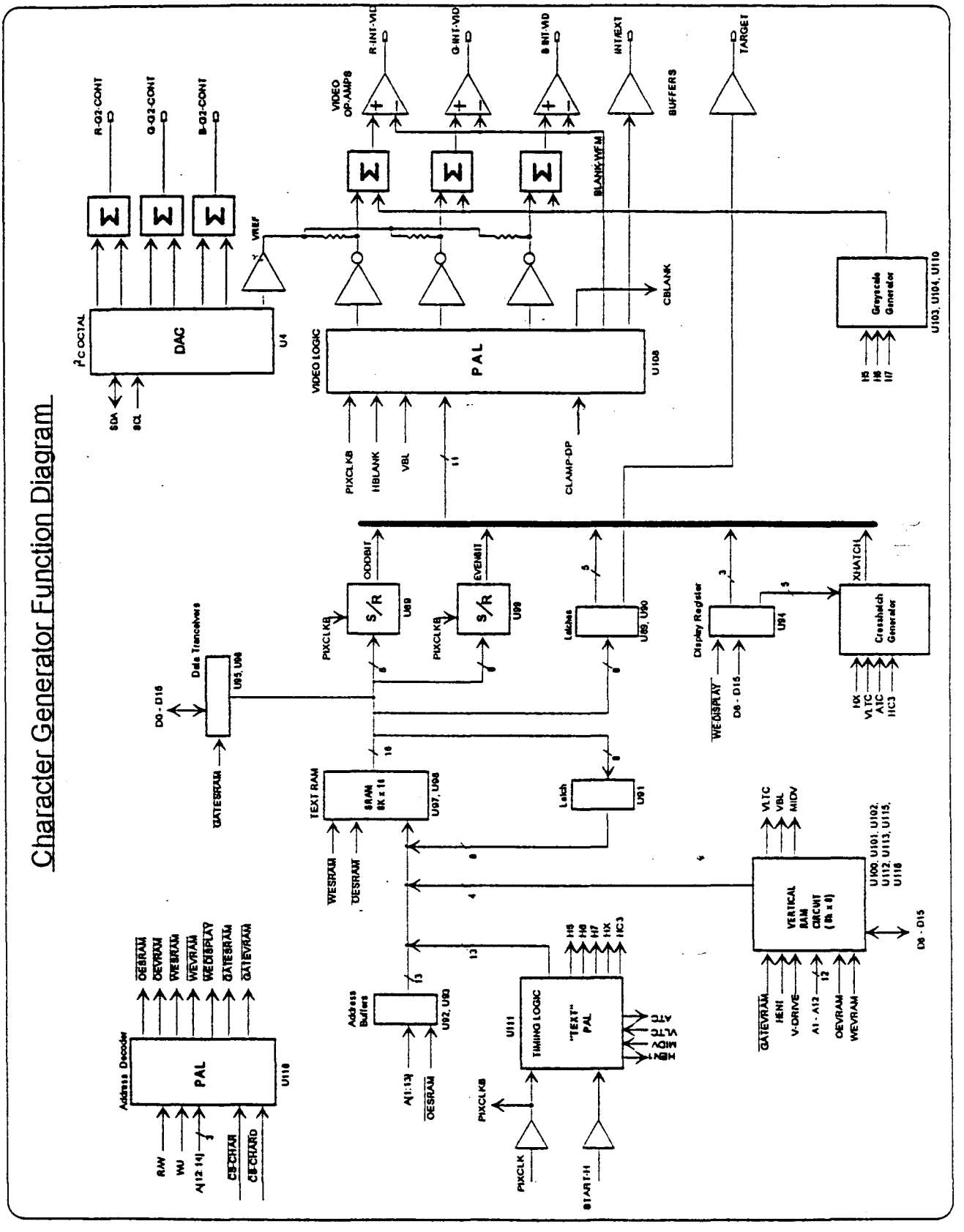


CPU Block Diagram




Waveform Generator Function Diagram
Convergence X 3
RH-CONV GH-CONV BH-CONV
RV-CONV GV-CONV BV-CONV
GH (GREEN ONLY)
GV (GREEN ONLY)
U400 U500 U600
U401 U501 U601
H-ALPHA
H-ALPHA-I
V-ALPHA
V-ALPHA-I
8 - Bit Latching DACS
U53, U54, U66
U52, U60, U70
U46, U59, U69
U47, U58, U68
OCTAL Latches
U50, U57, U67
U51, U62, U72
U54, U63, U73
HCLKA
HCLKB
VCLKA
VCLKB
HCLR
VCLR
U55, U64, U74
(Red + Blue only)
RH-FOCUS-PAR
GH-FOCUS-PAR
BH-FOCUS-PAR
U700
VREF
U78
U77
U76
(PARABOLA)
PROM
U85
U80
8PDT SWITCHES
H-SIZE
V-SIZE
I²C OCTAL DAC
U79
SDA
SCL
SRAM 2K X 8
U46, U65, U75
DATA TRANCEIVER
U66, U61, U71
D[8:15]
GATE
FOCUS WFM COUNTER
PAL
U82
CLK128B
START-FB
8 -BIT DAC
U37
U39
H - SIZE
V - SIZE
FET
ZERO - OUT
F/F
RESET
"ALPHA" ROM
U41
"WAVE" PAL
U48
RAMA[0:10]
ADDRESS BUFFERS
U41, U42
BUFFERS
ZONE LATCH
U40
Q[8:15]
WAVECLK
HI-FREQ
START-C
VDRIVE
CS-WAVE
A[1:11]
OE for each SRAM
WE for each SRAM
GATE for each SRAM
Address Decoder
PAL
U81, U83
R/W
WU
A[12:14]

Character Generator Function Diagram



2.0 Performance Specification

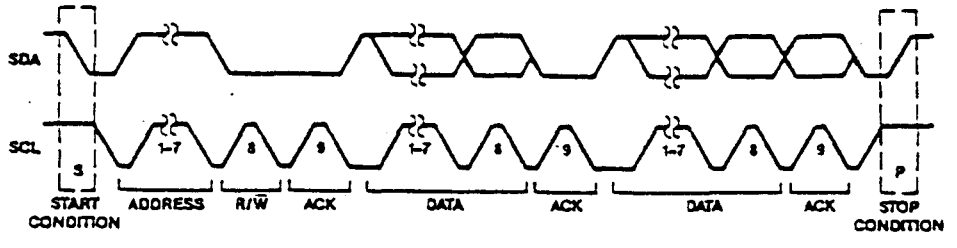
Signals input to and output from the CLM are described and specified in this section. The signals are grouped together according to function.

2.1 The I²C Bus

The I²C bus is a serial control bus which is used to communicate with and control other modules in the projector. It consists of two signals, SDA and SCL, which appear on backplane connector P1. SDA is bi-directional and carries data bits to and from the CLM. SCL outputs clock pulses during data transfers (one bit is transferred for each clock pulse). Devices attached to the bus must have open-drain or open collector outputs (there are pull-up resistors to +5V on the CLM). All devices must be "slaves", since SCL is implemented on the CLM as an output. Devices must not pull SCL low in order to interrupt a data transfer, as the CPU cannot respond properly. Important I²C bus specifications are listed below.

PARAMETER	MIN	MAX	UNIT
SCL clock frequency		100	kHz
Low period of the clock	4.7		us
High period of the clock	4.0		us
Rise time		1	us
Fall time		300	ns
Logic LOW level		1.5	Volts
Logic HIGH level	3.0		Volts
Bus capacitance		400	pF

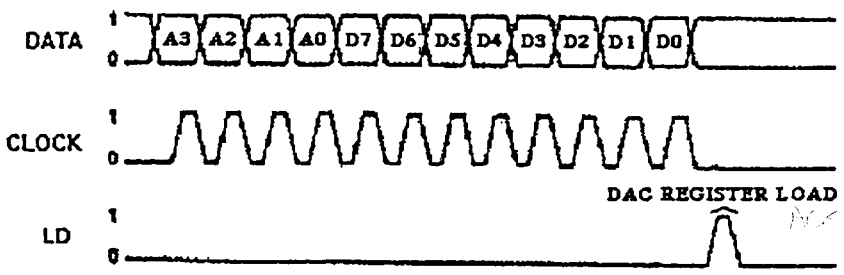
A data transfer cycle begins with a start condition and ends with a stop condition. A start condition is defined by a HIGH-to-LOW transition of SDA while SCL is HIGH. A stop condition is defined by a LOW-to-HIGH transition of SDA while SCL is HIGH. When data is not being transferred, both lines remain HIGH. Data is transferred in eight bit bytes. Each byte is followed by an acknowledge bit from the receiving device. Any number of bytes can be transmitted during a single data transfer cycle (ie. between start and stop conditions). Maximum transfer rate is 100 kbits/s. The actual transfer rate is software dependent. The timing of a data transfer is shown in the diagram below.



2.2 The DAC bus

The DAC bus consists of two HCMOS signals, DATA and CLOCK, which are output on backplane connector P1. In association with the I²C bus, these signals allow the CLM to load values into digital-to-analog converters (DACs) on other modules in the projector. Currently, the only type of device attached to the DAC bus is the Analog Devices DAC-8840, an octal 8-bit multiplying DAC. Data is loaded into this device by sequencing a 12-bit word on the DATA line. Each bit of data is clocked in with a low-to-high transition on the CLOCK line. The 12-bit word consists of a 4-bit address (A0-A3) to select the DAC channel, followed by an 8-bit data word (D0-D7). When all 12 bits have been clocked in, an active high strobe on the chip's LD (load) input writes the data into the selected channel. The LD pulse comes from an output of an I²C I/O port (PCF8574A) on the same module as the DAC. The output is toggled by software to create the LD pulse. When multiple DACs exist on the same module, each receives its own dedicated LD pulse.

The timing of a data transfer cycle is illustrated below. The clock rate is software dependent.



2.3 The Parallel Bus

The parallel bus is used to control optional cards inserted into the ACON and "spare" slots of the projector. The buses signals, which appear on backplane connector P1, originate from the 68000 microprocessor used in the CPU (see section 3.0 'Circuit Description'). The bus consists of address lines (A1-A16), data lines (D0-D15), bus control lines (RW, UDS*, LDS*, CS-ACON*, and CS-SPARE*), and other signals (ACON-RD, ACON-WR, ACON-I and RESET*). All signals are buffered HCMOS. when the cards are not being addressed, the address lines, data lines and bus control signals are inactive and are pulled either HIGH or LOW.

RW (read/write) is LOW during write cycles. LDS* (lower data strobe) is LOW when data is transferred on D0-D7. UDS* is LOW when data is transferred on D8-D15. Both LDS* and UDS* are LOW when 16-bit words are transferred on the bus. CS-ACON* and CS-SPARE* are active LOW chip selects for the ACON slot and "spare" slot, respectively.

ACON-RD, ACON-WR, ACON-I and RESET* support communication with a coprocessor on the ACON card. ACON-RD goes HIGH when the coprocessor reads data from the 68000. ACON-WR goes HIGH when the coprocessor writes data to the 68000. ACON-I goes high when either action occurs. RESET* goes LOW when the 68000 microprocessor is reset, serving to initialize the communication hardware on the ACON card.

2.4 Power Control Signals

Two outputs are used to control power in the projector. PWR-EN* is driven LOW to turn on both the low voltage power supply (LVPS) and the high voltage power supply (HVPS). HTR-STBY is driven LOW during power-on to switch the heater voltage for the CRTs from a standby voltage of 4.0V to the normal operating voltage of 6.3V. Both outputs are open-drain. Applicable logic levels for both are given below.

Logic LOW level:	0.8Vdc max
Logic HIGH level:	2.4Vdc min (unloaded)

The CLM routes power from the LVPS to several different devices in the projector. KEYPAD-PWR supplies power to the built-in keypad and IR-sensor. It also powers devices plugged into the REMOTE jack. CHIP-PWR supplies power to a chip (U1) on the Backplane Board.

KEYPAD-PWR	Voltage:	+12V +/-10%
	Current:	100 mA max (shared by IR-sensor, keypad and REMOTE jack)
CHIP-PWR	Voltage:	+5V +/- 5%
	Current:	25 mA max

2.5 Diagnostic Signals

Three diagnostic signals are input on backplane connector P1; EHT-FAIL, EHT-INHIBIT and CASE-COVER. The EHT-FAIL input is driven LOW when the HVPS comes on. The EHT-INHIBIT input is driven HIGH by a scan failure or an overcurrent condition. The CASE-COVER input is currently unsupported.

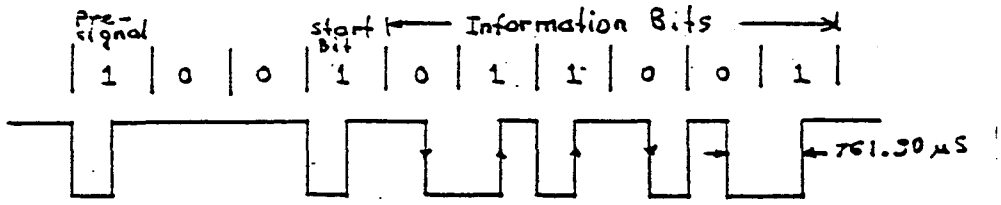
2.6 Keypad Inputs

The CLM receives user input from remote and built-in keypads. The KEYPAD and IR-SENSOR inputs on backplane connector P1 and the 'REMOTE' jack on the panel expect bi-phase encoded serial data with the following specifications:

Sub-carrier frequency:	35 kHz +/- 5 kHz (IR-SENSOR input expects no sub-carrier)
Main carrier period:	761.9 us
Packet length:	10 bits (4 preamble + 6 data)
Packet duration:	7.6 ms
Packet period:	46 ms
LOW level:	0.4V max
HIGH level:	5.0V min

Two different "protocols", A and B are supported. They are identified by the fourth bit of the 10-bit packet. The bit is 0 for protocol A and 1 for protocol B. (Note: Protocol A is identical in form to protocol 2 from B09 keypads. Likewise, protocol B is identical to protocol 1.)

A waveform (in protocol B) for the data code 011001 is shown below.



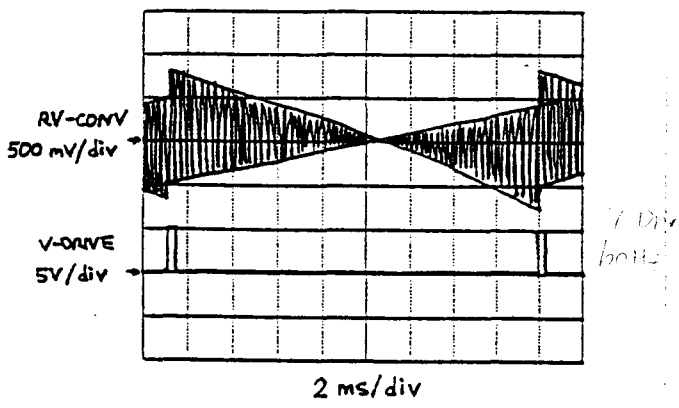
2.7 RS-232

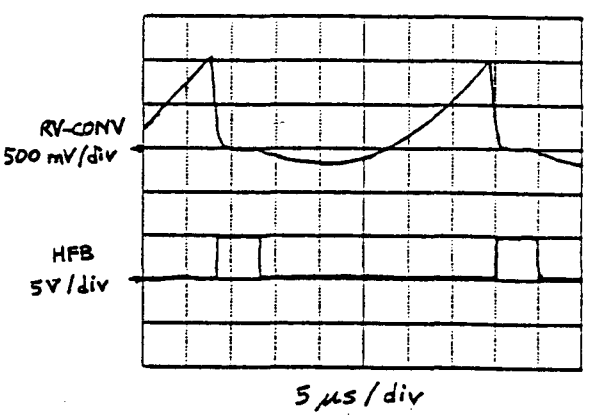
The CLM communicates bidirectionally with devices external to the projector using RS-232 via panel connectors J2, P3 are J3. Three wires - transmit, receive and ground - are required for connection. Hardware handshaking signals are not supported, therefore XON/XOFF flow control is required. Data format is 8 bits, 1 stop bit, no parity. The default baud rate for J2 and P3 is 9600 bps, but can be changed in a projector menu. The baud rate for J3 is fixed at 9600 bps. Signal levels are EIA-232D compatible, as follows:

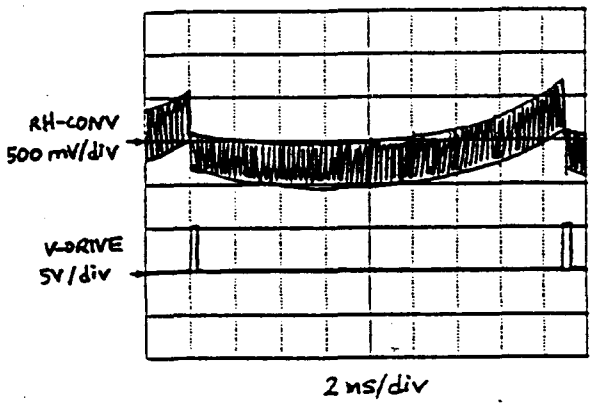
RS-232 Output	TxD HIGH:	+10V +/-5V
	TxD LOW:	- 10V +/-5V
RS-232 Input	RxD HIGH:	+3V min, +30V max
	RxD LOW:	- 3V max, - 30V min

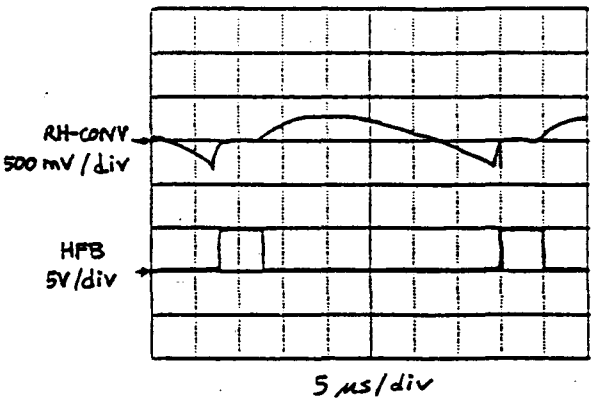
2.8 Convergence Waveforms

Six convergence waveforms are output on backplane connector P2; RH-CONV, RV-CONV, GH-CONV, GV-CONV, BH-CONV and BV-CONV. The shape of each waveform depends on the exact amounts of correction applied to the projected RGB component images. Typical horizontal and vertical correction waveforms for a fully-corrected image are shown below (6' diagonal image, 10 degree keystone, f_H = 31.5 kHz, f_V = 60 Hz). For each waveform, two diagrams are shown, one illustrating the horizontal component of the waveform and the other the vertical component.







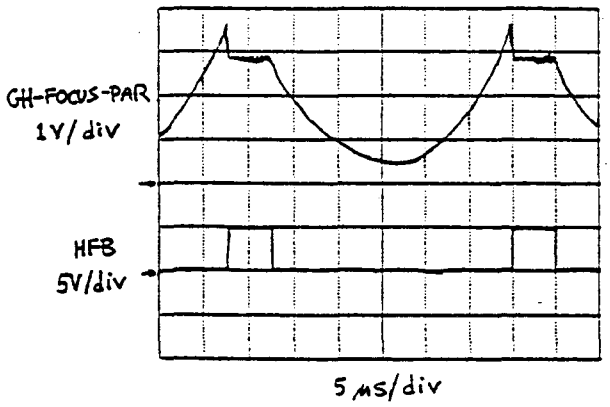


Signal levels are as follows (measured while loaded by the CVA):

Peak-to-peak voltage:	10Vp-p maximum
	2Vp-p typical (converged image)

2.9 Dynamic Focus Waveforms

Three horizontal-rate dynamic focus waveforms are output on backplane connector P2; RH-FOCUS-PAR, GH-FOCUS-PAR, and GH-FOCUS-PAR. Each waveform is essentially parabolic in shape. However, the amplitudes of the left and right sides of each parabola are independently adjustable under user control. A typical waveform is shown below (left side set to 50%, right side set to 100%).



Signal levels are as follows (measured while loaded by the FCM):

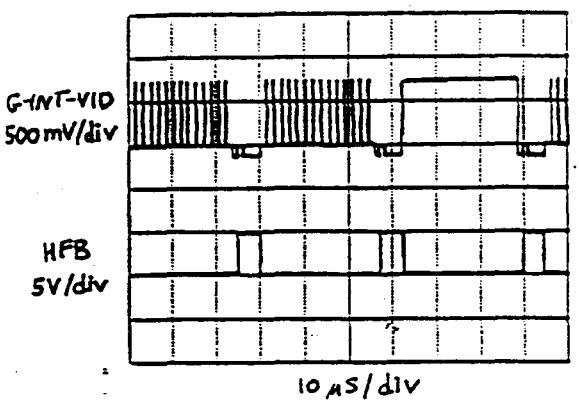
Peak-to-peak voltage:	3.5 Vp-p maximum

2.10 RGB Video

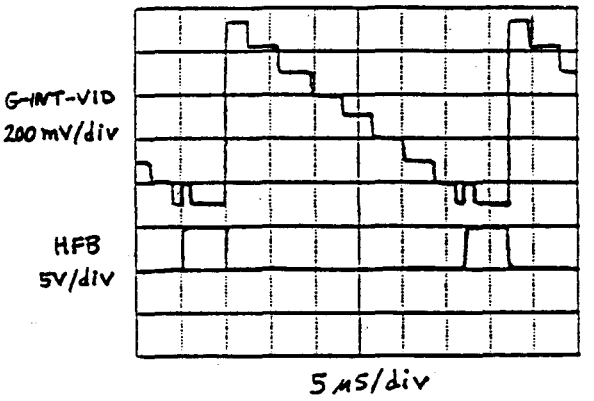
Three analog video signals are output on backplane connector P2; R-INT-VID, G-INT-VID and B-INT-VID. They are used by the VIM to display menus and test patterns. Each signal is terminated to 75 ohms on the VIM. Wveforms for the crosshatch and grayscale test patterns are shown below.

Peak-to-peak voltage:	1.0 Vp-p maximum
Peak video:	0.7V +/-5% above black level
Blacker-than-black:	100 mV below black level (typical)

CROSSHATCH

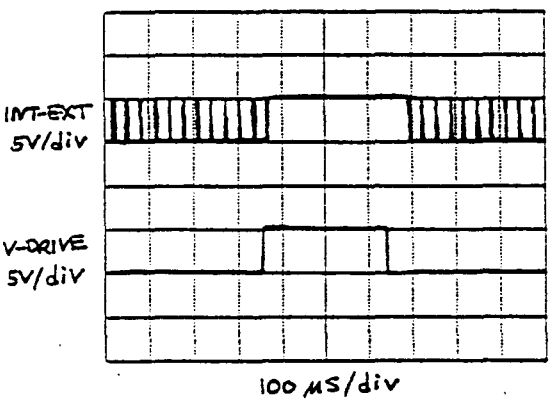


GRAYSCALE



2.11 INT-EXT

The INT-EXT signal, output on backplane connector P2, is used by the VIM to switch between internal and external video. This HCMOS signal goes HIGH when internal video is displayed, which includes the horizontal and vertical blanking intervals. The diagram below shows the behaviour of INT-EXT during the vertical retrace interval.



2.12 TARGET

The TARGET signal, output on backplane connector P2, is used by the optional ACON Board. This HCMOS signal goes HIGH to identify on-screen targets for the ACON sensor.

2.13 G2 Control Voltages

Three G2 control voltages are output on backplane connector P1; R-G2-CONT, G-G2-CONT, and B-G2-CONT. These voltages, in the range 0V - 10V, control grid 2 (G2) bias voltages in the range 0V-1000V from the HVPS. The voltage levels are set by software according to user-adjustable color temperature settings.

3.0 Circuit Description

The Control board is composed of three circuit blocks; the CPU, the Waveform Generator, and the Character Generator. The operation of each block is described in detail below.

3.1 CPU

The CPU circuitry contains two processors - a Motorola 68HC711D3 8-bit microcontroller (U16) and a Motorola 68000 16-bit microprocessor (U27). The microcontroller handles all serial input and output signals. It also outputs discrete control lines and monitors discrete control inputs. The 68000 runs the system software and interfaces with the Waveform Generator, the Character Generator and the DPB. The two processors communicate across a bi-directional 8-bit interface consisting of two latches for data transfer (U18, U20) and two flip-flops for handshaking (U9). Clock signals for both processors are provided by a 16 MHz crystal oscillator (U10) whose output is divided down to 8MHz by a flip-flop (U21).

The microcontroller and its support chips are powered from the +5V-STBY supply rail, which is present as soon as AC power is applied to the projector. The 68000 (and well as most of the Control Module) is powered from the +5V rail, which is not present until the Low Voltage Power Supply (LVPS) is turned on. This is done by the microcontroller in response to a "power-on" command from a hand-held keypad or from RS-232.

Because of the separate supply rails, the microcontroller and its support chips are kept electrically isolated from all other circuits when the LVPS is off. Signals which are not driven low or pulled low (open drain) by default are buffered by ICs U5 and U6, which are tristated by the signal PF (Power Fail) from undervoltage sensor U36.

3.1.1 Microcontroller

The 68HC711D3 is a single-chip microcontroller containing its own internal EPROM and RAM. On the Control Module, it is called the "I/O Processor" (IOP). All input and output is accomplished through four built-in 8-bit ports. This I/O capability is expanded by the addition of an external octal buffer (U19) and an octal latch (U7) connected to port C (C0-C7). The latch drives eight LEDs (LD1-LD8), which indicate the operational status of the projector. They are visible on the Control Module's panel. The buffer chip inputs diagnostic signals, some from other modules in the projector. (The specific function of each of the I/O ports is listed in Appendix A.)

Power-on reset of the microcontroller is handled by a "micromanager" IC (U17). When AC power is first applied to the projector, this IC ensures that the microcontroller is held in a reset state until the +5V-STBY supply rail stabilizes. The micromanager IC also allows a manual reset using a push-button (SW1) recessed into the Control Module's panel.

3.1.1.1 Power Control

When a "power-on" command is received from a hand-held keypad or RS-232, the microcontroller asserts PWR-EN* low to turn the low voltage and high voltage power supplies on. A secondary control signal, HTR-STBY, is also driven low to switch the heater voltage for the CRTs from a standby voltage of 4.0V to the normal operating voltage of 6.3V. Conversely, when a "power-off" command is received, PWR-EN* and HTR-STBY are driven high.

The PF signal from undervoltage sensor U36, input to the IOP through buffer U19, is monitored to verify the state of the low voltage power supply. When PF is low, the +5V rail is lower than 4.6V. If this is the case when the supply should be on, it may indicate an overload condition or an actual power supply failure.

3.1.1.2 Serial Control Buses

Two serial buses originate from the microcontroller; the Inter-Integrated-Circuit bus (I^2C) and the "DAC" bus. These are used to control remote I/O ports and digital-to-analog converters (DACs) on other modules in the projector. The I^2C bus is also used to access a small EEPROM on the projector's Backplane Board, which stores parameters during manufacture and setup of the projector. (This EEPROM is powered by +5V through R17 on the Control Board.)

The I^2C bus is composed of the SDA signal, carrying bi-directional serial data, and SCL, a clock signal. Both signals are buffered by open-drain inverters (U12) with local pull-up resistors to +5V. The DAC bus is composed of the DATA signal, which outputs data to the DACs, and CLOCK, which is toggled during data transfer. Both of these signals are HCMOS.

3.1.1.3 Keypad Input

The microcontroller receives and decodes serial data signals from three sources: the projector's built-in keypad, the projector's built-in IR sensor, and the 'REMOTE' jack (J1) on the Control module's panel. The built-in keypad and the IR-sensor are connected to the Backplane Board, from which the signals KEYPAD and IR-SENSOR are input to the CLM. The microcontroller also receives REMOTE-IN from J1, a signal which indicates the presence of a plug in the jack.

The built-in keypad, built-in IR-sensor, and REMOTE jack all draw power from the +12V-STBY supply rail. As with +5V-STBY, this voltage is present as soon as AC power is applied to the projector.

3.1.1.4 RS-232

The projector communicates with other devices using RS-232 via the "IN" and "OUT" connectors (J2 and P3 respectively) on the Control Module's panel. Cables attached to these connectors need only three wires; transmit, receive and ground. The transmit and receive signals are connected to an internal UART in the microcontroller through an RS-232 interface IC (U13) operating from +5V-STBY. A series of AND gates (U15) between the microcontroller and the interface IC allow the connection of multiple projectors in a "network", allowing any projector to talk to any other. The gates create two sets of transmit/receive pairs. One pair connects to a "down-linked" device (eg. another projector) via P3. The other pair connects to an "up-linked" device (another projector or a computer) via J2.

An additional RS-232 connector (J3) is provided for communication with a Marquee Signal Switcher. It is connected through another interface IC (U14) to a UART within the microcontroller on the DPB. When projector power is off, transmissions from the switcher are also routed, via U22, into the UART of the IOP microcontroller to listen for a "power-on" message. The IOP disconnects this signal from its UART when power is turned on.

3.1.1.5 Real Time Clock

A serial access clock chip (U8) provides a real time clock and calendar, as well as several bytes of non-volatile RAM for use by the microcontroller. The data in the chip is maintained in the absence of +5V-STBY power using a 3V lithium battery (B1). The RAM in the clock chip stores user-set communication parameters (RS-232 baud rate, etc) for access by the microcontroller when the projector is off.

3.1.2 68000 Microprocessor

The 68000 utilizes a 16-bit external data bus (D0-D15) and a 23-bit address bus. Only the first 19 address bits (A1-A19), defining a megabyte of address space, are used on the Control Board. This address space is decoded into several smaller ranges by ICs U28 and U30, which generate chip selects for all of the major circuits on the Control Board. (Refer to Appendix B for details of the address map.) ICs U1, U23, U24, U25 and U26 buffer the address, data and bus control signals for distribution off-board to the projector's expansion slots.

Power-on reset of the 68000 is handled by the microcontroller. When it asserts PWR-EN* low to turn on the power supplies, it also pulls RESET* low to hold the 68000 microprocessor in a reset state. When the supply voltages have stabilized, RESET* is pulled high and the microprocessor begins operation.

3.1.2.1 Memory

The projector's system software resides in a 16-bit EPROM (U35). Memory for stack space, variables and the projector's setup database is provided by two static RAMs (U31, U32). The content of the RAM chips is maintained in the absence of power using the 3V lithium battery (B1). The micromanager IC (U17) switches automatically to the battery when the +5V-STBY rail disappears, ensuring a continuous supply voltage (VBAT) to the RAM chips (and to clock chip U8). The micromanager IC also write-protects the RAM when switching to the battery. It accepts the chip select CS-RAM* and conditions it to produce CSTORAM*.

All data transfers by the 68000 are zero wait state, except those involving the Character Generator. Read or write access to the Character Generator during the visible portion of a video scan line results in the insertion of wait states, which delay the assertion of DTACK* from PAL U28 until a horizontal or vertical blanking interval occurs. This eliminates visible glitching of the on-screen image. Refer to section 3.1.2 of the Character Generator description for further details.

3.1.2.2 Interrupts

There are five interrupts sources; V-DRIVE, DPB-I, IOP-I, ACON-I, and TIMER (listed in order of decreasing priority). The V-DRIVE interrupt is created on the leading edge of the vertical drive pulse from the DPB. It marks the start of the vertical flyback interval. V-DRIVE is normally non-maskable, but becomes disabled when the NO-NMI signal from the microcontroller is driven high. The DPB-I, IOP-I, and ACON-I interrupts occur when one of the microcontrollers on the Control Board, DPB or expansion slot, respectively, communicates with the 68000. The TIMER interrupt is a periodic pulse from the microcontroller which is used as a time reference by the software.

The interrupts are captured by PAL U29 and encoded into the signals IPL0, IPL1 and IPL2, which are input to the 68000. On receipt of a valid code, the 68000 begins an interrupt cycle. An interrupt acknowledge signal, IACK*, is then created by U28 and input to the 68000 on the VPA* pin to identify the interrupt type as "autovector". U29 stores all pending interrupts and presents them in priority order to the 68000. Once serviced, a captured interrupt must be cleared by the 68000 before lower priority interrupts can be input to it. This is done by writing to the "interrupt capture register" in U29.

3.1.3 Coprocessor Interface

The 68000 and the microcontroller communicate across a bi-directional 8-bit parallel interface which allows asynchronous, full-duplex data transfers. Identical interfaces are used to communicate with microcontrollers on the DPB and the optional ACON board.

The interface uses two octal latches for data transfer (U18, U20) and two flip-flops for handshaking (U9). U20 latches a byte of data for transfer from the 68000 to the microcontroller. U18 latches a byte for transfer in the other direction. The latches are accessed by the microcontroller on port 'C' (C0-C7), and by the 68000 on the LSB of its data bus (D0-D7). The microcontroller strobes WR-TO-68000 low when it writes data into U18. It strobes RD-68000 low when it reads data from U20. Either action generates an interrupt, IOP-I, which is detected by U29. In response, the 68000 software reads the 'interrupt status register' (U11) to determine if a read or write occurred. Handshaking signals IOP-WR and IOP-RD input to U11 indicate the state of the flip-flops (U9). IOP-WR and READY (the inverse of IOP-RD) are monitored by the microcontroller to detect access to the latches by the 68000.

On power-up of the projector, and whenever a software reset instruction is processed by the 68000, the flip-flops are cleared by the RESET* signal. As a result, the latches appear "empty" to both processors.

3.2 Waveform Generator

The primary function of the Waveform Generator is to produce convergence correction waveforms which are amplified by the Convergence Amplifier (CVA) and applied to the convergence coils of the red, green and blue CRTs. These waveforms also allow correction of raster geometry, both "global" (top pincushion, bottom pincushion and bow) and "zonal" (green convergence). The Waveform Generator also produces three horizontal rate dynamic focus waveforms for the Focus Module (FCM), one for each CRT.

Six control signals generated by the DPB are input to the Waveform Generator; WAVE-CLKB, CLK128B, START-CB, START-FB, V-DRIVE and HI-FREQ. WAVE-CLKB is a clock signal used for the convergence waveforms. It has approximately 256 cycles in the active horizontal scan when the horizontal frequency is below 80 kHz, and only 128 cycles at or above 80 kHz. CLK128B is a clock signal with approximately 128 cycles in the active scan. START-CB is a pulse occurring once every scan line which determines when the convergence waveforms begin. It anticipates the start of scan by several hundred nanoseconds to compensate for delay in the convergence coils. START-FB is a similar pulse which determines the start of the focus waveforms. It also anticipates the start of scan to compensate for delay in the focus coils. V-DRIVE is the vertical drive pulse. It resets the Waveform Generator's counter circuitry at the end of each video field. Finally, HI-FREQ is a control signal that goes low when the scan frequency is at or above 80 KHz.

3.2.1 Convergence Waveforms

Six convergence waveforms are output from the Control Module; RH-CONV, RV-CONV, GH-CONV, GV-CONV, BH-CONV and BV-CONV. These allow the red, green and blue components of a projected image to be aligned on top of each other in the horizontal and vertical axes at multiple points on the raster. The waveforms are created by a hybrid digital/analog circuit. For every scan line in the raster, bytes of data are read sequentially from RAM and converted to analog. As the scan progresses from the top of the image to the bottom, the circuit smoothly interpolates from one waveform to another.

The circuitry can be divided into the following sections; RAM, the alpha circuit, and the output stage. These are described below.

3.2.1.1 RAM

Three static RAM chips hold nine rows of 64 correction values for each convergence waveform. RAM U46 stores data for red horizontal and red vertical. Similarily, U65 stores data for the green waveforms, and U75 stores data for blue. Convergence values are loaded into the RAMs by the 68000 microprocessor. PAL U81 decodes the address space defined by chip select CS-WAVE*, producing read and write control signals for each RAM (R-WE*, GATE-R*, G-WE*, GATE-G*, etc).

Each convergence value is a byte of data stored in offset binary form and accessed on the MSB of the 68000's data bus (D8-D15). Values in the range 00H to 7FH produce negative voltage excursions in the final waveform output. Values in the range 81H to FFH produce positive voltages. A value of 80H results in an output of zero volts.

The data bytes are continually read out of the RAMs by the convergence circuitry to produce the waveforms, interrupted only when the 68000 reads or writes convergence data (eg. during user adjustment). Counters implemented within U45, a programmable logic device (PLD), divide the active horizontal scan into 64 time slots (columns), and divide the raster into 8 vertical zones, each containing an equal number of scan lines. The nine rows of data stored in RAM for each waveform lie on the edges of each zone. U45 outputs a column address (RAMA0-RAMA5) and a zone address (RAMA6-RAMA9) to the RAMs. All three RAMs receive the same address from U45 in parallel, and thus output the waveform data in parallel.

Four accesses are made to the RAMs by U45 during each horizontal time slot; two for vertical correction data and two for horizontal correction data. RAMA10 indicates whether the values are vertical or horizontal. The first address of each pair fetches a data byte from each of the RAMs for the zone (n) containing the current scan line. The second address fetches a byte from each RAM at the same horizontal address, but from the following zone (n+1). Each pair of bytes goes to one of six "waveform channels", as described below in section 2.1.3.

The column address (RAMA0-RAMA5) is produced by an up-counter in U45 clocked by WAVE-CLKB. The count begins when a pulse on START-CB is received at the start of a scan line. At the end of the scan line, the counter is reset and data for the beginning of the next line is immediately accessed. This gives the analog output stage as much time as possible during horizontal retrace to slew to the new value before the next line begins.

For horizontal scan frequencies of 80 kHz or above, only the first 32 of the 64 values stored for each row are accessed by the column address. In this mode, the signal HI-FREQ is low, and the clock signal WAVE-CLKB generates only 128 cycles in the active scan, instead of 256. This reduces the rate at which data is accessed from RAM, allowing operation at very high scan frequencies.

3.2.1.2 Alpha Circuit

The nine rows of values stored in RAM for each convergence waveform apply directly only to nine scan lines which lie on the boundaries of the eight vertical zones defined by U45. Convergence values for every scan line between these boundaries are synthesized on the fly by the output stage circuitry using linear interpolation. The signals required for this interpolation are provided by the alpha circuit.

Each vertical zone contains 1/8 of the total number of visible lines in the raster. This number (N) is written into an 8-bit "Zone" latch (U40) by the microprocessor and is updated whenever the number of lines in the raster changes, ie. for new horizontal and/or vertical scan frequencies. The outputs of the latch (N0-N7) are input to PLD U45 and EPROM U44. A vertical counter in U45 counts down from 'N' to 0, decrementing by one each scan line, then back up to 'N'. This is repeated until the V-DRIVE pulse resets the counter, completing four cycles in each video frame. The outputs of the counter (I0-I7) form a number 'I' which is input to U44.

EPROM U44 is a look-up table which inputs 'N' and 'I' as addresses and outputs 'I/N' (I divided by N) as 8-bit data. 'N' is the number of scan lines in a vertical zone. 'I' is the number of lines from the start of the current zone (or the end, depending on the direction of the vertical counter) at which the current scan line occurs. Therefore, 'I/N' represents the fractional position of the current scan line within the current zone.

The outputs of U44 (I/N0-I/N7) are fed to digital-to-analog converters U37 and U39. U37 produces two complementary current outputs which are converted to voltages by U300 to create H-ALPHA and H-ALPHA-I. H-ALPHA is a voltage representation of 'I/N'. H-ALPHA-I represents it's inverse, '1-I/N'. They are triangle waveforms of opposite phase with four complete cycles in each video frame. Both waveforms are summed together to create a DC offset voltage H-ALPHA-REF. The outputs of U39 are similarly processed to create V-ALPHA, V-ALPHA-I, and V-ALPHA-REF. The peak voltages from U37 and U39 are set by H-SIZE and V-SIZE, respectively, from I^2C octal DAC U79. These control voltages are made to track changes in horizontal and vertical raster size in order to reduce misconvergence effects.

A circuit consisting of flip-flop U43 and FETs Q1 and Q2 forces HSIZE and VSIZE to zero during power-up of the projector. When RESET* is driven low to reset the 68000 microprocessor, the flip-flop is cleared. This causes the FETs to conduct, forcing the outputs of the DACs to zero. This in turn forces the final convergence waveform outputs to zero volts. The software then initializes all convergence RAM values to 80H and writes to the "Zone" latch (U40). This strobes WR-NLATCH* low, which toggles the flip-flop and turns the FETs off, restoring the outputs of the DACs. This procedure prevents random waveforms from being output to the CVA before the RAMS can be initialized, which could cause excessive current draw from the amplifiers.

3.2.1.3 Output Stage

The output stage consists of six "waveform channels", two for each color. Each channel is composed of two latches, two 8-bit multiplying DACs and a quad op-amp IC. The circuits for the channels are nearly identical, therefore only the red horizontal channel will be described in detail.

Horizontal convergence data from the red RAM (U46) are input to latches U50 and U51. The output of U50 feeds multiplying DAC U53. Similarily, the output of U51 feeds DAC U52. Each DAC contains a transparent latch. Both DACs are loaded with new data every horizontal time slot in the following manner:

Consider a time slot divided into 4 equal parts - 1/4, 2/4, 3/4 and 4/4. During 1/4, a convergence value for the zone containing the current scan line is clocked into latch U50 on the rising edge of HCLKA. During 2/4, the convergence value for the next zone is clocked into latch U51 on the rising edge of HCLKB. During 3/4 and 4/4, the write-enable pulse HCLK* is driven low. The bytes in the two latches are simultaneously loaded into the DACs on the rising edge of HCLK* at the end of the 4/4 interval. Clock signals HCLK*, HCLKA and HCLKB are generated by U45.

By using the waveforms H-ALPHA and H-ALPHA-I from the "alpha" circuit, the two DACs solve the interpolation equation,

$$C = (I/N) * A + (1-I/N) * B,$$

where 'C' is the final output voltage, 'A' is the convergence value in one DAC, and 'B' is the value in the other DAC. The 'I/N' and '1-I/N' terms are represented by H-ALPHA and H-ALPHA-I, respectively. The data in U53 (A) is multiplied by H-ALPHA, which is input as the DAC's reference voltage. The data in U52 (B) is similarily multiplied by H-ALPHA-I. The resulting voltages are summed together in U400. H-ALPHA-REF is also added to ensure a bipolar output.

A smooth interpolation between the 'A' value at the start of a zone and the 'B' value at the start of the next zone occurs because H-ALPHA and H-ALPHA-I are complementary waveforms. At the start of a zone, one voltage is full scale, while the other is zero. The full-scale voltage ramps linearly down to zero, decreasing by a small increment on each scan line. The other voltage ramps up to full scale in a similar manner, so that by the end of the zone, the voltage levels have reversed.

To reduce the effects of gain and offset errors in the DACs, the 'A' and 'B' values alternate between the two DACs every zone. On even zones, 'A' is loaded into U53 and 'B' is loaded into U52. On odd zones, 'A' is loaded into U52 while 'B' is loaded into U53. This ensures that a new value is loaded into a DAC only when its reference voltage is zero, eliminating the possibility of an abrupt voltage change or "basketweave" artifact.

DACs U47 and U48 create the red vertical convergence waveform in a similar manner, using V-ALPHA, V-ALPHA-I and V-ALPHA-REF, and timing signals VCLKA, VCLKB, and VCLK*. Vertical convergence values are clocked into latches U47 and U48 during intervals 3/4 and 4/4, respectively. The data are then clocked into the DACs at the end of the 2/4 interval.

The green and blue waveform channels are similar to the red waveform channels. To support "global" and zonal geometry corrections, the green vertical waveform (GV) is added to both the red and blue vertical waveforms. Similarly, the green horizontal waveform (GH) is added to the red and blue horizontal waveforms. Horizontal rate parabolas generated in software are loaded into the vertical half of the green RAM to allow user adjustment of top pincushion, bottom pincushion and bow.

3.2.2 Dynamic Focus Waveforms

The Waveform Generator outputs three horizontal rate waveforms; RH-FOCUS-PAR, GH-FOCUS-PAR, and BH-FOCUS-PAR. These waveforms are used by the FCM for dynamic focus correction of the red, green and blue CRTs, respectively. (Vertical dynamic focus waveforms are created by the VDM.)

The waveforms are created digitally. A counter (PAL U82) outputs an address to a PROM (U85) containing a parabola look-up table. The PROM outputs 8-bit data to three multiplying DACs (U76, U77, U78). As a result, the DACs output parabolic waveforms during each scan line. The amplitude of each waveform is controlled by a pair of voltages from an I^2C octal DAC (U79), one pair for each waveform. One voltage controls the amplitude on the left side of the waveform and the second controls the amplitude on the right side of the waveform. The voltages are switched in the middle of each scan line by toggling a triple analog switch (U80) with the most significant bit of the count.

3.3 Character Generator

The Character Generator creates text and test patterns for on-screen display. Text is used for menus, help pages, slidebars and other visual elements of the projector's user interface. Test patterns are provided to aid in setup of the projector. The Character Generator also generates G2 control voltages for the red, green and blue CRTs.

Eight signals created by the Character generator are output from the Control Module. Red internal video (R-INT-VID), green internal video (G-INT-VID), blue internal video (B-INT-VID), and INT-EXT are sent to the Video Input Module (VIM). The VIM uses INT-EXT to switch the displayed image between internal and external video on a pixel-by-pixel basis. The TARGET signal is output to the optional ACON module. It goes high to identify characters used as targets by the ACON sensor. R-G2-CONT, G-G2-CONT, and B-G2-CONT are G2 control voltages for the red, green and blue CRTs, respectively. They are sent to the High Voltage Power Supply (HVPS) which generates the actual G2 voltages.

The Character Generator inputs five control signals generated by the DPB; PIXCLKB, START-HB, V-DRIVE, CLAMP-DP and HBLANK. PIXCLKB is a clock signal with approximately 256 cycles in the active scan. It is used to create the video pixels. START-HB is a pulse occurring once every scan line which determines where the video signals start on the left edge of the image. V-DRIVE is the vertical drive pulse. It resets the character generator's counter circuitry at the end of each video field. CLAMP-DP is a pulse created within the horizontal flyback interval. It controls when video clamping occurs. Finally, HBLANK is the horizontal blanking pulse.

3.3.1 Text

Text is displayed on a 64 column by 24 row matrix. The location of each character on the screen is mapped to an address in RAM. A 16-bit word is stored for each screen location. The least significant byte, stored in RAM U97, specifies one of 256 available characters (letters, numbers, graphics symbols, etc.) for display. The most significant byte, stored in RAM U98, specifies how the character will look (eg. its color). It is called the "attribute" byte. To display a screen of text, the 68000 microprocessor writes the appropriate codes into the RAMs for each screen location. The 68000 accesses the RAMs through buffers U92, U93, U95 and U96. PAL U118 decodes the address space defined by chip select CS-CHAR* (and a delayed version CS-CHARD*) to provide the required read and write control signals.

Half of the RAM space is allocated for the screen map. The other half stores bitmaps for all 256 possible characters. These are permanently stored in EPROM U35 and copied into the RAMs by the 68000 at projector power-up. Each bitmap is 8 pixels wide by 16 pixels tall, stored as 16 words. Only the most significant byte of each word is displayed. The most significant bit of this byte is the first pixel scanned out to the display.

Pixels are either "off" (0) or "on" (1). Their appearance on-screen is determined by the attribute byte stored for each screen location. "Off" pixels normally appear black while "on" pixels display one of eight colors (red,

green, blue, cyan, magenta, yellow, black or white). "Off" pixels can be made "transparent", displaying the external video instead of black. A character can also be displayed "inverse", in which the "on" and "off" pixels are reversed. It is also possible to mix transparent mode with inverse mode so that "on" pixels display the external video.

PLD U111 provides timing signals required to scan the characters out to the display. It contains an up-counter clocked by PIXCLKB, which divides the active horizontal scan time into 64 time slots (columns). It also contains a vertical counter clocked by VLTC from the vertical RAM circuit (described below), which divides the raster into 24 rows. During the first half of each horizontal time slot, U111 generates a column address (CG0-CG5) and a row address (CG6-CG11), which together specify one of the screen locations. CG12 is low to address the lower half of RAM space. In response to this address, RAMs U97 and U98 each output a byte. One byte (the attribute byte) is clocked into latch U89 using FONT-CLK. The other byte is clocked into latch U91.

During the second half of the horizontal time slot, the data in U91 is fed back to the RAMs on CG4-CG11. In addition, CG12 goes high to address the upper half of the RAM space. Together, these bits address one of the character bitmaps. Address bits CG0-CG3 from the vertical RAM circuit (described below) specify which line of pixels in the bitmap will be displayed on the current scan line. In response to this new address, RAMs U97 and U98 each output another byte. These are loaded into shift registers U88 and U99 using LOADSHIFT*. At the same moment, the attribute byte in U89 is latched into U90. This ensures that a character's attributes take effect at the same time its pixels are shifted out to the display.

3.3.1.1 Vertical RAM Circuit

The vertical RAM circuit is composed of a 12-bit counter (U114), a RAM (U102), a latch (U101), and several buffers (U100, U112, U113, U115, U116). The counter generates an address for the RAM which is incremented every scan line. Therefore, one unique byte is output from the RAM for every scan line in the raster. The RAM is loaded by the 68000 microprocessor on the MSB of its data bus (D8-D15).

The four most significant bits from the RAM are multiplexed onto address lines CG0-CG3 by buffer U100 during the second half of a horizontal time slot. These address bits select which of the sixteen bytes in a character's bitmap will be displayed on a given scan line in the raster. The bits in each byte are loaded by the 68000 with values that ensure a uniform appearance of the characters regardless of the number of scan lines in the raster. If there are more scan lines in the raster than the number of rows times the number of bytes in each bitmap (24 X 16 = 384), then some bytes are repeated over several scan lines. This is done to preserve the size and on-screen position of the text rows. For the same reason, if there are less than 384 scan lines in the raster, some bytes are omitted.

The four least significant bits from RAM U102 are clocked into latch U101. As the raster lines are scanned down the screen, the individual bits create digital waveforms. The waveform VLTC is a clock signal which increments the row counter in U111 once for each row of text. VBL is the vertical blanking waveform, which is affected by user-settings for top blanking and bottom blanking. The screen is blanked when VBL is high. The waveform MIDV marks the exact middle of the raster. It is used by the grayscale test pattern circuit.

3.3.1.2 Output Circuit

The bytes loaded into shift registers U88 and U99 during a given horizontal time slot are shifted out by clock signal PIXCLKB during the next time slot. The resulting pixel streams, ODDBIT from U88 and EVENBIT from U99, are input to PAL U108. Here they are interleaved such that EVENBIT is displayed only during the first half of each PIXCLKB cycle and ODDBIT is displayed during the second half. Two pixels are therefore output for every clock cycle. The pixels are also logically conditioned by the attribute bits from U90. RED-ATT, GREEN-ATT, and BLUE-ATT specify the color of the "on" pixels. A low INVERSE bit reverses what is displayed for "on" and "off" pixels. A high TRANSPARENT bit allows external video to be displayed during "off" pixels.

Three video pixel streams are output from U108, one each for red, green and blue. They are buffered by open drain inverters in U104, which convert a CMOS high logic level to an analog video level controlled by VREF from I²C octal DAC U4. The resulting video signals are amplified by U105, U106 and U107 and output from the Control Module with 2X gain at 75 ohms impedence. These signals, R-INT-VID, G-INT-VID and B-INT-VID, are sent to the VIM.

Register U94 controls what the projector will display on-screen. The register is loaded by the 68000 microprocessor on the MSB of its data bus (D8-D15). Outputs W0, W1 and W2 control the width of crosshatch lines (described in section 3.2 below). The TEXTON-OFF bit turns text display off when it is low. Outputs SELECT0, SELECT1, and SELECT2 form a code determining what is displayed "behind" the text (ie. the background). These bits are input to PAL U108 for selecting between a black screen, white screen, test pattern or external video for output. Refer to Appendix C for details.

The INT-EXT signal from U108 controls fast analog switches on the VIM, which are used to switch the displayed image between internal and external video on a pixel-by-pixel basis. INT-EXT is driven high to display internal video. This allows "windows" of text (eg. a slidebar) to be overlayed onto the external video. For example, when a menu is displayed, INT-EXT is high for the part of each scan line which contains the menu, and low for the rest of the visible image.

The INT-EXT signal is also used to blank the edges of the raster. The vertical blanking signal VBL from U101 and the horizontal blanking signal HBLANK from the DPB are combined in U108 with the clamping pulse CLAMP-DP from the DPB. This creates the waveform BLANK-WFM, which is subtracted from the RGB video signals in the output amplifiers. The internal video is thus driven to black when a clamping pulse occurs and "blacker-than-black" during the remainder of the blanking intervals. At the same time, INT-EXT is driven high to display internal video, thereby blanking the display.

To prevent visible "glitching" of the image when the 68000 accesses RAM in the Character Generator, a composite blanking signal CBLANK is created in U108 and input to PAL U28. CBLANK is formed by ORing VBL and CLAMP-DP. Any access to register U94 or RAMs U97, U98 or U102 by the 68000 while CBLANK is low (ie. during active video scan) results in the insertion of wait states which delay the start of data transfer. When CBLANK goes high during a blanking interval, U28 is allowed to assert DTACK* and complete the read or write cycle. Chip selects CS-CHAR* and CS-CHARD* are likewise delayed. This prevents "glitches" on the screen which would otherwise occur when a 68000 access interrupts the transfer of pixel data from the RAMs into the shift registers. The glitches are restricted to the blanking intervals when they cannot be seen.

3.3.2 Test Patterns

In addition to text, the Character Generator produces a variety of different test patterns. It generates three different crosshatches - a "plain" crosshatch, a dense crosshatch and a crosshatch with a dot in the center of each square. It generates a dot field, which is useful for stigmator setup. It also generates a grayscale pattern, which is useful during color temperature setup.

Crosshatch and dot patterns are created with a circuit consisting of a PAL (U117) and a delay line (U109). Horizontal and vertical counter outputs from PLD U111 are ANDed in the PAL to create a crosshatch and ORed to create dots. The delay line allows the width of vertical lines (and of dots) to be controlled.

Horizontal lines in the crosshatch are single scan lines whose on-screen position is defined by ATC from U111 and VLTC from the vertical RAM. Vertical lines are created from signals HX and HC3 from U111. The HX signal is composed of 32 narrow pulses on every scan line. Each pulse is high for one half of a single PIXCLKB cycle. HX is input to delay line U109, which outputs several versions of the pulse train, delayed by integer multiples of 5 nsec. These signals are input to PAL U117, which selects one of the pulse trains according to a code formed by W0, W1 and W2 from register U94. The delayed pulses are ORed with the undelayed pulses. This narrows the width of the pulses, resulting in theinner vertical lines. The width is chosen by software according to the horizontal scan frequency.

SELECT0 and SELECT1 from register U94 are input to U117 to select the specific crosshatch or dot pattern that will be output. The resulting signal, XHATCH, is input to PAL U108 and mixed with pixels from the shift registers in the text generation circuit.

The grayscale pattern is generated by a circuit consisting of OR gates (U103), open drain inverters (U104), a precision R2R resistor ladder and a video amplifier (U110). The circuit produces an eight level stairstep which reverses direction half way down the raster. PLD U111 outputs HCOUNT5*, HCOUNT6* and HCOUNT7*, which are the three most significant bits of the horizontal count. These are gated in U103 by a blanking signal from U108, which disables the counter outputs when text is being displayed on top of the grayscale pattern. The counter outputs are converted to video levels by the open drain inverters. A weighted sum is then performed by the R2R ladder. The resulting voltage stairstep is amplified by U110 and added equally to the red, green and blue video signals from PAL U108. To reverse the direction of the stairstep midway down the raster, the counter signals are inverted by signal MIDV from the vertical RAM.

3.3.3 G2 Control Voltages

The High Voltage Power Supply (HVPS) provides voltages in the range of 0 - 1000V to each of the CRTs. These voltages bias grid 2 (G2) of the electron gun in each CRT and must be adjusted so that black portions of the video signal appear black on-screen. The Character Generator outputs three control voltages, R-G2-CONT, G-G2-CONT, and B-G2-CONT, in the range 0 - 10V to allow these adjustments.

The control voltages are produced by an I^2C 6-bit octal DAC (U4). To ensure fine adjustment resolution, two channels are used for each control voltage. They are summed in a 64:1 ratio into op-amp U200 to approximate 12 bits of resolution. A stable reference voltage is provided by regulator U2. The regulator's +12V output is also used as a reference for DACs U37 and U39 in the convergence waveform circuit.

4.0 Power Consumption

The power consumption figures given below for the Control Module are maximums, measured at 130 kHz in a Marquee 9000 with the Stigmator Waveform Board attached. They include the power consumption of the Deflection Processor Board. (Note: The current draw on +5V decreases as scan frequency decreases.)

VOLTAGE	TOLERANCE	CURRENT
+5V	+/- 5%	2.9 A
-5V	+/- 5%	40 mA
+15V	+/- 5%	150 mA
-15V	+/- 5%	120 mA

5.0 Test and Alignment

- to be added

6.0 Mechanical Specifications

Module Dimensions (L x W x H)	9.00" x 9.75" x 1.25"
Panel Dimensions (L x W)	10.56" x 1.5"

7.0 Appendices

Appendix A: I/O Processor Ports

(a) 68HC711D3 Built-in Ports

Name	Pin	I/O	Function
PA0	30	I	IR sensor input
PA1	29	I	Remote keypad input (via panel jack J1)
PA2	28	I	Built-in keypad input
PA3	27	O	Enable switcher output into UART (active high)
PA4	26	O	Timer interrupt to 68000
PA5	25	O	Chip select for Real Time Clock (active high)
PA6	24	O	Serial clock for Real Time Clock
PA7	23	I/O	Serial Data (bidirectional) for Real Time Clock
PB0	39	O	68000 reset (active high)
PB1	38	O	NMI disable (active high)
PB2	37	O	Power enable (active high)
PB3	36	O	Heater standby (active low)
PB4	35	O	LED register load pulse (active high)
PB5	34	O	Input buffer enable (active low)
PB6	33	O	Write pulse to 68000 latch (active low)
PB7	32	O	Read pulse to 68000 latch (active low)
PC0	3	I/O	Parallel Data I/O (Bit 0) LSb
PC1	4	I/O	Parallel Data I/O (Bit 1)
PC2	5	I/O	Parallel Data I/O (Bit 2)
PC3	6	I/O	Parallel Data I/O (Bit 3)
PC4	7	I/O	Parallel Data I/O (Bit 4)
PC5	8	I/O	Parallel Data I/O (Bit 5)
PC6	9	I/O	Parallel Data I/O (Bit 6)
PC7	10	I/O	Parallel Data I/O (Bit 7) MSb
PD0	16	I	RS-232 input (receive)
PD1	17	O	RS-232 output (transmit)
PD2	18	O	DAC bus serial data output
PD3	19	O	DAC bus serial clock output
PD4	20	O	I2C serial clock output (inverted)
PD5	21	O	I2C serial data output (inverted)
PD6	13	I	I2C serial data input (non-inverted)
PD7	12	---	unused

(b) Port C Expansion

U7, LED Register:

Bit	Pin	Description
PC0	2	Power-on (green)
PC1	5	Standby (yellow)
PC2	6	Error (red)
PC3	9	LVPS fail (red)
PC4	12	EHT fail (red)
PC5	15	Horiz. fail (red)
PC6	16	Vert. fail (red)
PC7	19	'C' (red)

U19, Input Buffer:

Bit	Pin	Description
PC0	2	high if remote plugged into J1
PC1	4	EHT-INHIBIT (active high)
PC2	6	EHT-FAIL (active high)
PC3	8	low if +5V power rail < 4.6V
PC4	11	case cover interlock
PC5	13	not used (tied low)
PC6	15	high if U18 holds unread data
PC7	17	low if U20 holds unread data

Appendix B: 68000 Address Map

(a) General Address Map

Address Range	Chip Select	Device
00000 - 7FFFF	CS-ROM*	EPROM
80000 - 9FFFF	CS-RAM*/CSTORAM*	RAM
A0000 - BFFFF	CS-SPARE*	Spare slot
C0000 - C7FFF	U30 pin 15	Interrupt capture register (U29)
C8000 - CFFFF	CS-STAT*	Interrupt status register (U11)
D0000 - D7FFF	CS-IOP*	I/O Processor (IOP)
D8000 - DFFFF	CS-DPB*	Deflection Processor Board (DPB)
E0000 - E7FFF	CS-WAVE*	Waveform Generator
E8000 - EFFFF	CS-CHAR/CS-CHARD*	Character Generator
F0000 - F7FFF	CS-ACON*	ACON module
F8000 - FFFFF	n/a	unused

(b) Convergence Circuit Address Map

Address Range	Function
E0000 - E07FF	Red Horizontal - 16 rows of 64 values (stored in MSB of word), organized as follows: E0000 Row 1, value 1 E003E Row 1, value 64 E0040 Row 2, value 1, etc...
E0800 - E0FFF	Red Vertical - organized same as red horizontal
E1000 - E17FF	Green Horizontal
E1800 - E1FFF	Green Vertical
E2000 - E27FF	Blue Horizontal
E2800 - E2FFF	Blue Vertical
E3000 - E3FFF	Zone Latch

(c) Character Generator Address Map

Address Range	Function
E8000 - E9FFF	Screen Space - 32 rows of 64 characters, organized as follows: E8000 Row 1, column 1 E807E Row 1, column 64 E8080 Row 2, column 1, etc...
EA000 - EAFFF	Font Space - 256 characters, organized as follows: EA000 Character 1, slice 1 EA01E Character 1, slice 16 EA020 Character 2, slice 1, etc...
EC000 - EDFFF	Display register
EE000 - EFFFF	Vertical RAM

Appendix C: Registers

(a) Interrupt Capture Register (C0000)

Bit	Interrupt	Level	Source
D7	V-DRIVE	7	leading edge of VFB
D6	DPB-I	6	Deflection Processor Board (DPB)
D5	IOP-I	5	I/O Processor (IOP)
D4	ACON-I	4	ACON processor
D3	TIMER	3	timer (from IOP)

Notes: 1) Interrupts with smaller levels have lower priority.
2) Writing a binary 1 to a bit clears the associated interrupt. Writing a binary 0 to a bit has no effect.

(b) Interrupt Status Register (C8000)

Bit	Signal	Description
0	DPB-WR	DPB write
1	DPB-RD	DPB read
2	IOP-WR	IOP write
3	IOP-RD	IOP read
4	ACON-WR	ACON write
5	ACON-RD	ACON read
6	n/a	reserved - tied low
7	n/a	reserved - tied low

Notes: 1) A high "write" input indicates unread data from the device.
2) A high "read" input indicates that the device has read the last byte sent to it.

(c) Display Register (EC000)

Bit	Function
D8	Text display bit (high = text on)
D9	Background mode - bit 0
D10	Background mode - bit 1
D11	Background mode - bit 2
D12	unused
D13	Crosshatch line width - bit 0
D14	Crosshatch line width - bit 1
D15	Crosshatch line width - bit 2

Background Display Modes:

D11	D10	D9	Mode
0	0	0	Dense crosshatch
0	0	1	Crosshatch
0	1	0	Dot field
0	1	1	Crosshatch with dots
1	0	0	White field
1	0	1	Grayscale
1	1	0	External video
1	1	1	Black field

Crosshatch Line Width:

D15	D14	D13	Delay (ns)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	15
1	0	0	20
1	0	1	25
1	1	0	30
1	1	1	30

Appendix D: Character Generator Control Codes

(a) Attribute Byte

Bit	Function
D8	Character color - red bit
D9	Character color - green bit
D10	Character color - blue bit
D11	reserved - set low
D12	reserved - set high
D13	Transparency bit (active high)
D14	Inverse bit (active low)
D15	ACON bit (active high)

Character Color:

D10	D9	D8	Color
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White

Inversion and Transparency:

D14	D13	"ON" Pixels	"OFF" Pixels
0	0	black	character color
0	1	background video	character color
1	0	character color	black
1	1	character color	background video

(b) Vertical RAM Output

Bit	Output	Function
D8	VLTC	Row counter clock (active high strobe)
D9	VBL	Vertical blanking (active high)
D10	VCRST	unused
D11	MIDV	Middle of raster (high = second half of raster)
D12	VDAT4	Font slice address - bit 0 (lsb)
D13	VDAT5	Font slice address - bit 1
D14	VDAT6	Font slice address - bit 2
D15	VDAT7	Font slice address - bit 3 (msb)

Notes: 1) The row counter strobe is delayed in the circuit by two scan lines (ie. the row counter will increment two lines after the scan line selected in the vertical RAM.)
2) VBL transitions are delayed by one scan line.
3) The MIDV transition is delayed by two scan lines.
4) The font slice address is NOT delayed.

Appendix E: Control Module Panel

Panel features are listed in left-to-right order as viewed from the rear of the projector.

"RESET" Switch

This momentary push-button switch is recessed to prevent accidental activation. It rests the 68HC11 microcontroller, which responds by turning the projector off and waiting for a "power-on" message.

"POWER" LED

This green LED illuminates after the power supplies have been turned on and the power-up sequence of the projector is complete. It is normally the only LED that is lit during projector operation.

"STANDBY" LED

This amber LED illuminates after the power cord is connected to the projector to indicate the projector's readiness to be turned on. The LED turns off when the projector is powered up. As a second function, the "STANDBY" LED also lights when the projector has been placed in STANDBY mode (sound and picture disabled). In this mode, the green "POWER" LED is also illuminated.

Diagnostic LEDs

These red LEDs illuminate to indicate a malfunction that may prevent correct operation of the projector. The meaning of each LED is indicated below:

"ERROR"	- indicates an error or malfunction within the control system (memory or checksum error, I^2C error, etc.)
"LVPS"	- lights if the low voltage power supply requires servicing
"EHT"	- lights if the high voltage power supply requires servicing
"H. FAIL"	- lights if horizontal scan has failed.
"V. FAIL"	- lights if vertical scan has failed.
"C"	- for future use

"REMOTE" Jack

This miniature stereo phone jack can be used to connect a wired keypad or a remote IR sensor to the projector.

RS-232 "IN" and "OUT" Connectors

These nine-pin D connectors allow connection of multiple projectors in a network and/or control of one or more projectors by RS-232 from a computer. A computer would be connected to the "IN" connector (female), while the "OUT" connector (male) would be used to network to additional projectors (by going to the next projector's "IN" connector, and so on).

Switcher Connector

This female nine-pin D connector allows communication with one or more optional Marquee Signal Switchers.

Appendix F: PLD Design Files

Printouts of the design files for the programmable logic devices on the Control Board are attached. The design descriptions are in PALASM format.

```
;PALASM Design Description

;---------------------------- Declaration Segment --------------------

TITLE     GLUE21 - Glue Logic for 68000 Microprocessor
PATTERN   U28 of Control Module
REVISION  2.1
AUTHOR    Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      May 9, 1993

CHIP  GLUE  PALCE22V10

;---------------------------- Description Segment --------------------
;
; The GLUE pal provides several functions for the 68000 system that
; serve to "glue" it together:
;
;    - chip select generation (active low) for the program EPROM,
;      the battery-backed RAM chips, the SPARE slot, the external bus
;      buffers, the convergence circuit and the character generator.
;
;    - data-transfer-acknowledge (DTACK) generation (active low) for
;      the 68000.  All data transfers are zero wait state except those
;      involving the character generator.  Read or write access to the
;      character generator during a video scan will result in the
;      insertion of wait states until a horizontal or vertical blanking
;      interval occurs.  This prevents glitching of the screen.
;
;    - interrupt acknowledge signal (IACK) generation (active low)
;      for inputting to the VPA pin of the 68000 in response to
;      interrupts captured by U29. This enables autovectoring.
;
;
; Revision History
;
;    1.X - all 1.X versions were based on a 16V8 device
;    2.0 - first version for 22V10
;    2.1 - deleted wait state insertion for convergence circuit
;          (did not work - needs additional delays)
;
;---------------------------- PIN Declarations -----------------------

PIN   1    8M          COMBINATORIAL ; INPUT  8 MHz clock
PIN   2    CBLANK      COMBINATORIAL ; INPUT  composite blanking signal
PIN   3    CS_CHARI    COMBINATORIAL ; INPUT  "raw" char gen chip select
PIN   4    AS_         COMBINATORIAL ; INPUT  68k address strobe
PIN   5    FC0         COMBINATORIAL ; INPUT  68k function code bit0
PIN   6    FC1         COMBINATORIAL ; INPUT  68k function code bit1
PIN   7    FC2         COMBINATORIAL ; INPUT  68k function code bit2
PIN   8    CS_WAVEI    COMBINATORIAL ; INPUT  "raw" conv. chip select
PIN   9    A16         COMBINATORIAL ; INPUT  68k address bit
PIN   10   A17         COMBINATORIAL ; INPUT  68k address bit
PIN   11   A18         COMBINATORIAL ; INPUT  68k address bit
PIN   12   GND
PIN   13   A19         COMBINATORIAL ; INPUT  68k address bit
PIN   14   DTACKDLY       REGISTERED ; OUTPUT delayed DTACK
PIN   15   DTACK       COMBINATORIAL ; OUTPUT data transfer acknowledge
PIN   16   IACK        COMBINATORIAL ; OUTPUT interrupt acknowledge
PIN   17   CS_ROM      COMBINATORIAL ; OUTPUT EPROM chip select (U35)
PIN   18   CS_RAM      COMBINATORIAL ; OUTPUT RAM chip select (U31,U32)
PIN   19   CS_EXT      COMBINATORIAL ; OUTPUT external bus buffer select
PIN   20   CS_SPARE    COMBINATORIAL ; OUTPUT SPARE slot select
PIN   21   CS_WAVE     COMBINATORIAL ; OUTPUT convergence chip select
```

```
PIN  22   CS_CHAR   COMBINATORIAL ; OUTPUT char gen chip select
PIN  23   CS_CHARD     REGISTERED ; OUTPUT delayed CS_CHAR
PIN  24   VCC

;---------------------------- Boolean Equation Segment -------------

EQUATIONS

/CS_ROM = /A19 * /AS

/CS_RAM = A19 * /A18 * /A17 * /AS

/CS_SPARE = A19 * /A18 * A17 * /AS

/CS_EXT = A19 * A18 * A17 * A16 * /AS
        + /CS_SPARE

/IACK = FC0 * FC1 * FC2 * /AS

DTACKDLY = /CBLANK * DTACKDLY * /AS
         + AS

/DTACK = /AS * /FC0 * CS_CHARI
       + /AS * /FC1 * CS_CHARI
       + /AS * /FC2 * CS_CHARI
       + /DTACKDLY * /CS_CHARI

CS_WAVE = CS_WAVEI

CS_CHAR = CS_CHARI + DTACKDLY

CS_CHARD = CS_CHAR


;---------------------------- Simulation Segment --------------------

SIMULATION


TRACE_ON FC0 FC1 FC2 IACK AS 8M CS_CHARI CS_CHAR DTACKDLY DTACK CBLANK

SETF /AS /FC2 /FC1 /FC0 A19 /A18 /CBLANK CS_CHARI CS_WAVEI

CLOCKF 8M
SETF  /AS /FC2 FC1 /FC0

CLOCKF 8M
SETF  /AS FC2 /FC1 /FC0

CLOCKF 8M
SETF  /AS FC2 FC1 /FC0

CLOCKF 8M
SETF  /AS FC2 FC1 FC0

CLOCKF 8M
SETF AS FC2 FC1 FC0

CLOCKF 8M
SETF /AS /FC2 /FC1 /FC0 A18 /CS_CHARI

CLOCKF 8M
SETF /AS
```

```
CLOCKF 8M
SETF /AS

CLOCKF 8M
SETF /AS

CLOCKF 8M
SETF CBLANK

CLOCKF 8M
SETF /AS

CLOCKF 8M
SETF AS

CLOCKF 8M
SETF AS

CLOCKF 8M
SETF /AS

CLOCKF 8M
SETF /CBLANK

CLOCKF 8M
SETF /AS

CLOCKF 8M
SETF AS CS_CHARI

CLOCKF 8M
SETF AS

CLOCKF 8M
SETF AS

TRACE_OFF

;-----------------------------------------------------------------
```

```
;PALASM Design Description

;------------------------- Declaration Segment ---------------------

TITLE     INTER12 - Interrupt Controller for 68000
PATTERN   U29 of Control Board
REVISION  1.2
AUTHOR    Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      01/26/93

CHIP  INTER  PALCE610

;------------------------- Description ----------------------------
;
; This IC captures interrupts and inputs them to the 68000. There
; are five interrupt sources:
;
;          Interrupt  Level  IPL Code  Priority
;
;            VDRIVE     7      000     highest
;            DPB        6      001       -
;            IOP        5      010       -
;            ACON       4      011       -
;            TIMER      3      100     lowest
;
; The VDRIVE interrupt occurs on the leading edge of the active-high
; VDRIVE (V-DRIVE) signal from the DPB. It is normally non-maskable,
; but becomes disabled when NO_NMI (NO-NMI) from U16 (68HC711D3
; microcontroller) is driven high. The DPB, IOP and ACON interrupts
; indicate a read from or write to the 68000 by the DPB, IOP (U16)
; or ACON hardware, respectively. TIMER interrupts are generated at
; 10 msec intervals by U16 for use by the 68000 software.
;
; U29 individually and asynchronously captures interrupts from all
; five sources (on low-to-high transitions) and encodes them with a
; priority encoder, creating IPL2, IPL1 and IPL0 (the IPL code)
; which are input to the 68000. On receipt of a code other than 111,
; the 68000 begins an interrupt cycle. An interrupt acknowledge
; signal (IACK*) is then created by U28 and input to the 68000 on its
; VPA* pin. This allows an "autovector" to occur. U29 stores the
; interrupts and presents them in priority order to the 68000. The
; 68000 software is responsible for clearing captured interrupts
; immediately after responding to them by writing to an "interrupt
; capture" register in U29. This will strobe the active low register
; select input CS_INT (CS-INT*).
;
;
; Revision History:
;
;   V1.0 - original
;
;   V1.1 - Modified priority encoder to block VDRIVE code (000) when
;          NO_NMI is high, eliminating the possiblility of a noise
;          pulse creating a non-maskable interrupt during power-up.
;
```

```
;--------------------------- PIN Declarations ----------------------

PIN  1      CLK1                          ; INPUT  not used
PIN  2      TIMER       COMBINATORIAL     ; INPUT  TIMER interrupt from IOP
PIN  3      Q4          REGISTERED        ; OUTPUT captured ACON interrupt
PIN  4      Q3          REGISTERED        ; OUTPUT captured TIMER interrupt
PIN  5      ACON_I      COMBINATORIAL     ; INPUT  ACON interrupt
PIN  6      IOP_I       COMBINATORIAL     ; INPUT  IOP interrupt
PIN  7      DPB_I       COMBINATORIAL     ; INPUT  DPB interrupt
PIN  8      IPL2        COMBINATORIAL     ; OUTPUT interrupt code - bit 2
PIN  9      IPL1        COMBINATORIAL     ; OUTPUT interrupt code - bit 1
PIN  10     IPL0        COMBINATORIAL     ; OUTPUT interrupt code - bit 0
PIN  11     VFB_I       COMBINATORIAL     ; INPUT  VFB interrupt
PIN  12     GND
PIN  13     CLK2                          ; INPUT  N/C
PIN  14     CS_INT      COMBINATORIAL     ; INPUT  capture register select
PIN  15     Q5          REGISTERED        ; OUTPUT captured IOP interrupt
PIN  16     Q6          REGISTERED        ; OUTPUT captured DPB interrupt
PIN  17     Q7          REGISTERED        ; OUTPUT captured VFB interrupt
PIN  18     D7          COMBINATORIAL     ; INPUT  68000 data bit
PIN  19     D6          COMBINATORIAL     ; INPUT  68000 data bit
PIN  20     D5          COMBINATORIAL     ; INPUT  68000 data bit
PIN  21     D4          COMBINATORIAL     ; INPUT  68000 data bit
PIN  22     D3          COMBINATORIAL     ; INPUT  68000 data bit
PIN  23     NO_NMI      COMBINATORIAL     ; INPUT  NMI disable from IOP
PIN  24     VCC

;--------------------------- Boolean Equation Segment --------------

EQUATIONS

Q3 = VCC
Q3.CLKF = TIMER
Q3.RSTF = D3 * /CS_INT

Q4 = VCC
Q4.CLKF = ACON_I
Q4.RSTF = D4 * /CS_INT

Q5 = VCC
Q5.CLKF = IOP_I
Q5.RSTF = D5 * /CS_INT

Q6 = VCC
Q6.CLKF = DPB_I
Q6.RSTF = D6 * /CS_INT

Q7 = VCC
Q7.CLKF = VFB_I * /NO_NMI
Q7.RSTF = D7 * /CS_INT

IPL0 = /((Q3 * /Q4 * /Q6)
     + (Q5 * /Q6)
     + Q7 * /NO_NMI)

IPL1 = /((Q3 * /Q4 * /Q5)
     + Q6
     + Q7 * /NO_NMI)

IPL2 = /(Q4
     + Q5
     + Q6
     + Q7 * /NO_NMI)
```

```
;------------------------ Simulation Segment ---------------------

SIMULATION

TRACE_ON VFB_I NO_NMI DPB_I IOP_I ACON_I TIMER D7 D6 D5 D4 D3 CS_INT
         IPL0 IPL1 IPL2

;Initialize Inputs
SETF /D3 /D4 /D5 /D6 /D7 CS_INT NO_NMI /VFB_I /DPB_I /IOP_I /ACON_I
     /TIMER

;Simulation Sequence
SETF VFB_I               ;VFB interrupt
                         ;not captured since NO_NMI signal is asserted
SETF /VFB_I /NO_NMI      ;deassert NO_NMI
SETF VFB_I               ;VFB interrupt again
                         ;captured and output
SETF /VFB_I DPB_I        ;DPB interrupt
                         ;captured but not output since VFB event pending
SETF /DPB_I D7
SETF /CS_INT             ;clears VFB event
                         ;now DPB code is output
SETF CS_INT IOP_I        ;IOP interrupt
                         ;captured but not output since DDP event pending
SETF /IOP_I /D7 D6
SETF /CS_INT             ;clears pending DPB event
                         ;now IOP code is output
SETF CS_INT ACON_I       ;ACON interrupt
                         ;captured but not output since IOP event pending
SETF /ACON_I /D6 D5
SETF /CS_INT             ;clears pending IOP event
                         ;now ACON code is output
SETF CS_INT TIMER        ;Timer interrupt
                         ;captured but not output since ACON event pending
SETF /D5 D4
SETF /CS_INT             ;clears pending ACON event
                         ;now Timer code is output
SETF CS_INT /D4 D3
SETF /CS_INT             ;clears Timer event
SETF CS_INT

;simulation done

TRACE_OFF

;-----------------------------------------------------------------------
```

```
;PALASM Design Description

;------------------------ Declaration Segment ------------------------

TITLE     CPU11 - Convergence Circuit Address Decoder
PATTERN   U81 of Control Board
REVISION  1.1
AUTHOR    Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      May 3, 1992

CHIP   CPU   PALCE16V8

;------------------------ Descriptions ------------------------------
;
; This IC allows access by the 68000 to the convergence circuit RAM
; (U46, U65, and U75) and the "Zone" latch (U40). Chip select CS_WAVE
; (CS-WAVE*) from U28 is strobed low for accesses in the address range
; E0000-EFFFE. This address range is decoded as follows:
;
;      E0000 - E0FFE     Red RAM (U46)
;      E1000 - E1FFE     Green RAM (U65)
;      E2000 - E2FFE     Blue RAM (U75)
;      E3000 - E3FFE     Zone latch (U40)
;
; The PAL outputs write enable signals for the three RAMs and the latch,
; as well as direction signals for the RAM tranceivers (U49, U61, U71).
; The register (U40) is write-only.
;
; Revision History:
;
;   V1.0 - original
;   V1.1 - clean-up of equation syntax in design file - no actual
;          change to content of JEDEC file
;
;------------------------ PIN Declarations --------------------------

PIN   1    CLK           COMBINATORIAL ; INPUT  N/C
PIN   2    CS_WAVE       COMBINATORIAL ; INPUT  convergence chip select
PIN   3    RW            COMBINATORIAL ; INPUT  CPU read/write signal
PIN   4    WU            COMBINATORIAL ; INPUT  CPU UDS* gated by R/W
PIN   5    I4            COMBINATORIAL ; INPUT  N/C
PIN   6    A12           COMBINATORIAL ; INPUT  CPU address bit
PIN   7    A13           COMBINATORIAL ; INPUT  CPU address bit
PIN   8    A14           COMBINATORIAL ; INPUT  CPU address bit
PIN   9    I8            COMBINATORIAL ; INPUT  N/C
PIN   10   GND
PIN   11   OE            COMBINATORIAL ; INPUT  output enable (test only)
PIN   12   IO0           COMBINATORIAL ; OUTPUT N/C
PIN   13   R_WE          COMBINATORIAL ; OUTPUT write enable for U46
PIN   14   G_WE          COMBINATORIAL ; OUTPUT write enable for U65
PIN   15   B_WE          COMBINATORIAL ; OUTPUT write enable for U75
PIN   16   WR_NLATCH     COMBINATORIAL ; OUTPUT write enable for U40
PIN   17   GATE_R        COMBINATORIAL ; OUTPUT U49 xcvr direction
PIN   18   GATE_G        COMBINATORIAL ; OUTPUT U61 xcvr direction
PIN   19   GATE_B        COMBINATORIAL ; OUTPUT U71 xcvr direction
PIN   20   VCC
```

```
;------------------------- Boolean Equation Segment --------------------
EQUATIONS
/WR_NLATCH = /CS_WAVE * /RW * /WU * A12 * A13 * /A14
/R_WE = /CS_WAVE * /RW * /WU * /A12 * /A13 * /A14
/G_WE = /CS_WAVE * /RW * /WU * A12 * /A13 * /A14
/B_WE = /CS_WAVE * /RW * /WU * /A12 * A13 * /A14
/GATE_R = /CS_WAVE * /A12 * /A13 * /A14
/GATE_G = /CS_WAVE * A12 * /A13 * /A14
/GATE_B = /CS_WAVE * /A12 * A13 * /A14
IO0 = GND
;------------------------- Simulation Segment ------------------------
SIMULATION
TRACE_ON A14 A13 A12 RW WU CS_WAVE
WR_NLATCH R_WE G_WE B_WE GATE_R GATE_G GATE_B
SETF /A14 /A13 /A12 RW WU /CS_WAVE
SETF /A14 A13 /A12
SETF /A14 A13 A12
SETF CS_WAVE
SETF /CS_WAVE
SETF /RW
SETF /WU
SETF WU A13 /A12
SETF /WU
SETF WU /A13 A12
SETF /WU
SETF WU /A13 /A12
SETF /WU
SETF WU
SETF CS_WAVE
TRACE_OFF
;-----------------------------------------------------------------------
```

```
;PALASM Design Description

;---------------------- Declaration Segment ----------------------

TITLE     FOCUS20 - Focus Waveform Counter
PATTERN   U82 of Control Board
REVISION  2.0
AUTHOR    Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      May 6, 1993

CHIP   FOCUS   PALCE22V10

;---------------------- Description ------------------------------
;
; This device is configured as a 7-bit synchronous counter whose
; outputs drive a PROM (U85) programmed with a parabola waveform.
; The 8-bit PROM data is input to three 8-bit registered DACs (U76,
; U77, U78) which output horizontal dynamic focus waveforms for the
; red, green and blue CRTs.  The most significant bit of the count
; (F6) is also fed to a triple bilateral switch (U80) which
; alternates between left side and right side reference voltages for
; each of the DACs.  A WE_DAC signal loads data into the DAC
; registers 64 times each scan line.
;
; Changes from earlier versions:
;
;  All previous versions (1.X) were based on a 16V8 device.
;
;---------------------- PIN Declarations -------------------------

PIN   1     CLK128B     COMBINATORIAL ; INPUT   clock signal
PIN   2     START_FB    COMBINATORIAL ; INPUT   waveform start pulse
PIN   3     I3          COMBINATORIAL ; INPUT   N/C
PIN   4     I4          COMBINATORIAL ; INPUT   N/C
PIN   5     I5          COMBINATORIAL ; INPUT   N/C
PIN   6     I6          COMBINATORIAL ; INPUT   N/C
PIN   7     I7          COMBINATORIAL ; INPUT   N/C
PIN   8     I8          COMBINATORIAL ; INPUT   N/C
PIN   9     I9          COMBINATORIAL ; INPUT   N/C
PIN   10    I10         COMBINATORIAL ; INPUT   N/C
PIN   11    I11         COMBINATORIAL ; INPUT   N/C
PIN   12    GND
PIN   13    OE          COMBINATORIAL ; INPUT   output enable (test only)
PIN   14    F0             REGISTERED ; OUTPUT  counter output- LSB
PIN   15    F5             REGISTERED ; OUTPUT  counter output
PIN   16    F4             REGISTERED ; OUTPUT  counter output
PIN   17    F3             REGISTERED ; OUTPUT  counter output
PIN   18    F2             REGISTERED ; OUTPUT  counter output
PIN   19    F1             REGISTERED ; OUTPUT  counter output
PIN   20    F6             REGISTERED ; OUTPUT  counter output- MSB
PIN   21    FTC            REGISTERED ; OUTPUT  focus terminal count
PIN   22    ENF            REGISTERED ; OUTPUT  end of focus count
PIN   23    WE_DAC      COMBINATORIAL ; OUTPUT  write enable for DACs
PIN   24    VCC
```

```
;------------------------ Boolean Equation Segment -----------------

EQUATIONS

;         TOGGLES                          RETAINS COUNT

F6 = ENF*(/F6*F0*F1*F2*F3*F4*F5  +F6*(/F0+/F1+/F2+/F3+/F4+/F5))
F5 = ENF*(/F5*F0*F1*F2*F3*F4     +F5*(/F0+/F1+/F2+/F3+/F4))
F4 = ENF*(/F4*F0*F1*F2*F3        +F4*(/F0+/F1+/F2+/F3))
F3 = ENF*(/F3*F0*F1*F2           +F3*(/F0+/F1+/F2))
F2 = ENF*(/F2*F0*F1              +F2*(/F0+/F1))
F1 = ENF*(/F1*F0                 +F1*(/F0))
F0 = ENF*/F0

FTC = /F0 * F1 * F2 * F3 * F4 * F5 * F6

ENF = (START_FB + ENF) * /FTC    ; starts on START_FB, ends on FTC

F0.TRST = /OE
F1.TRST = /OE
F2.TRST = /OE
F3.TRST = /OE
F4.TRST = /OE
F5.TRST = /OE
F6.TRST = /OE
FTC.TRST = /OE
ENF.TRST = /OE

WE_DAC = /F0

WE_DAC.TRST = /OE

;------------------------ Simulation Segment ----------------------

SIMULATION

TRACE_ON CLK128B ENF WE_DAC F0 F1 F2 F3 F4 F5 F6 FTC OE

PRELOAD /ENF

SETF /CLK128B /OE /START_FB

CLOCKF CLK128B

SETF START_FB

CLOCKF CLK128B

SETF /START_FB

FOR X := 1 TO 126 DO
BEGIN
CLOCKF CLK128B
END

FOR X := 1 TO 5 DO
BEGIN
CLOCKF CLK128B
END

SETF OE

TRACE_OFF
```

```
;PALASM Design Description

;---------------------- Declaration Segment ------------------------------

TITLE     COLOR13 - Pixel Processor
PATTERN   U108 of Control Board
REVISION  1.3
AUTHOR    Joel Tarback, Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      01/27/93

CHIP  COLOR  PAL22V10 ; --- MUST use Lattice (10 ns) ---

;---------------------- Description ---------------------------------------
;
; This PAL inputs character pixel streams OD (ODDBIT) and EV (EVENBIT)
; from shift registers U88 and U99, as well as XH (XHATCH) from pal
; U117, processes them and outputs digital RGB video. It also inputs
; blanking and clamp signals and outputs several composite blanking
; waveforms.
;
; ODDBIT and EVENBIT are interleaved such that EVENBIT is displayed only
; during the first half of each PIXCLKB cycle and ODDBIT is displayed
; during the second half. Two pixels are therefore output for every clock
; cycle. The pixels are modified by attribute bits which are stored for
; each character. RED-ATT, GREEN-ATT, and BLUE-ATT select the color of "on"
; (binary 1) pixels. These colors are simply the eight possible binary
; combinations of red, green, and blue. The INVERSE and TRANSPARENT bits
; modify the pixels as follows:
;
;          INVERSE  TRANSPARENT  "On" pixels  "Off" pixels
;          -------  -----------  -----------  ------------
;             0          0          black         color
;             0          1        background      color
;             1          0          color         black
;             1          1          color       background
;
; S0 (SELECT0), S1 (SELECT1) and S2 (SELECT2) from register U94 select the
; type of background video to be displayed in the transparent portions
; of the characters. When external video is chosen, the /EXT (INT-EXT)
; output is driven low. This signal controls analog switches on the VIM.
;
; Vertical blanking signal VBL and horizontal blanking signal HBLANK are
; combined with CLAMP (CLAMP-DP) to create BLANK_WFM (BLANK-WFM), which is
; subtracted from the RGB video signals in the output amplifiers (U105,
; U106 and U107). This drives the video to black when a clamping pulse
; occurs and "blacker-than-black" during the rest of the blanking
; intervals. INT-EXT is driven high during the blanking intervals to
; show the internal video and thus blank the display.
;
; CBLANK, created from CLAMP (CLAMP-DP) and VBL, is output to PAL U28.
; If CBLANK is low, U28 will insert wait states into any access made to
; register U94 or RAMs U97, U98 or U102 by the 68000. The read or write
; cycle is thus delayed until CBLANK goes high during a horizontal or
; vertical blanking interval. This prevent "glitching" of the display.
; Design note: CLAMP-DP is used because it occurs inside the true
; horizontal blanking interval. If HBLANK were used, completion of a
; 68000 cycle would glitch the far left side of the display.
;
```

```
;---------------------- PIN Declarations ---------------------------------

PIN   1  CLK       COMBINATORIAL ; INPUT  pixel clock (PIXCLKB) from DPB
PIN   2  CLAMP     COMBINATORIAL ; INPUT  CLAMP-DP pulse from DPB
PIN   3  XH        COMBINATORIAL ; INPUT  XHATCH test pattern from U117
PIN   4  EV        COMBINATORIAL ; INPUT  EVENBIT from shift register U99
PIN   5  OD        COMBINATORIAL ; INPUT  ODDBIT from shift register U88
PIN   6  R         COMBINATORIAL ; INPUT  RED-ATT - red color attribute
PIN   7  G         COMBINATORIAL ; INPUT  GREEN-ATT - green color attribute
PIN   8  B         COMBINATORIAL ; INPUT  BLUE-ATT - blue color attribute
PIN   9  C0        COMBINATORIAL ; INPUT  TRANSPARENT attribute (active hi)
PIN   10 C1        COMBINATORIAL ; INPUT  INVERSE attribute (active low)
PIN   11 S0        COMBINATORIAL ; INPUT  S2-S0 - background selection
PIN   12 GND                               code, as follows:
PIN   13 S1        COMBINATORIAL ; INPUT    0XX = one of 4 xhatch patterns
PIN   14 S2        COMBINATORIAL ; INPUT    100 = white field
                                 ;          101 = grayscale
                                 ;          110 = external video
                                 ;          111 = black field
PIN   15 VBL       COMBINATORIAL ; INPUT  vertical blanking waveform
PIN   16 /EXT      COMBINATORIAL ; OUTPUT internal/external video select
PIN   17 /GRAY     COMBINATORIAL ; OUTPUT turns on grayscale generator
PIN   18 /BLUE     COMBINATORIAL ; OUTPUT blue digital video
PIN   19 /GREEN    COMBINATORIAL ; OUTPUT green digital video
PIN   20 /RED      COMBINATORIAL ; OUTPUT red digital video
PIN   21 HBLANK    COMBINATORIAL ; INPUT  horizontal blanking wfm from DPB
PIN   22 BLNK_WFM  COMBINATORIAL ; OUTPUT video blanking waveform BLANK-WFM
PIN   23 CBLANK    COMBINATORIAL ; OUTPUT composite blanking wfm for U28
PIN   24 VCC

;---------------------- Boolean Equation Segment -------------------------

EQUATIONS

GREEN = /HBLANK */VBL*(/CLK*(C1*/OD*G+/C1*OD*G + /S2*C1*/C0*OD*XH
        + /S2*/C1*/C0*/OD*XH + S2*/S1*/S0*C1*/C0*OD
        + S2*/S1*/S0*/C1*/C0*/OD) + CLK*(C1*/EV*G + /C1*EV*G
        + /S2*C1*/C0*EV*XH + /S2*/C1*/C0*/EV*XH
        + S2*/S1*/S0*C1*/C0*EV + S2*/S1*/S0*/C1*/C0*/EV))

BLUE = /HBLANK*/VBL*(/CLK*(C1*/OD*B + /C1*OD*B + /S2*C1*/C0*OD*XH
       + /S2*/C1*/C0*/OD*XH + S2*/S1*/S0*C1*/C0*OD
       + S2*/S1*/S0*/C1*/C0*/OD) + CLK*(C1*/EV*B + /C1*EV*B
       + /S2*C1*/C0*EV*XH + /S2*/C1*/C0*/EV*XH
       + S2*/S1*/S0*C1*/C0*EV + S2*/S1*/S0*/C1*/C0*/EV))

RED = /HBLANK*/VBL*(/CLK*(C1*/OD*R +/C1*OD*R +/S2*C1*/C0*OD*XH
      + /S2*/C1*/C0*/OD*XH + S2*/S1*/S0*C1*/C0*OD
      + S2*/S1*/S0*/C1*/C0*/OD) + CLK*(C1*/EV*R +/C1*EV*R
      + /S2*C1*/C0*EV*XH + /S2*/C1*/C0*/EV*XH
      + S2*/S1*/S0*C1*/C0*EV + S2*/S1*/S0*/C1*/C0*/EV))

GRAY = /HBLANK*/VBL*(/CLK*(S2*/S1*S0*/C1*/C0*/OD + S2*/S1*S0*C1*/C0*OD)
       + CLK*(S2*/S1*S0*/C1*/C0*/EV + S2*/S1*S0*C1*/C0*EV))

EXT = /HBLANK*/VBL*(/CLK*(S2*S1*/S0*/C1*/C0*/OD + S2*S1*/S0*C1*/C0*OD)
      + CLK*(S2*S1*/S0*/C1*/C0*/EV + S2*S1*/S0*C1*/C0*EV))

BLNK_WFM = /CLAMP * (HBLANK + VBL)

CBLANK = CLAMP + VBL
```

```
;---------------------- Simulation Segment ------------------------------

SIMULATION

TRACE_ON S0 S1 S2 C0 C1 EV OD CLK XH R RED EXT GRAY CLAMP HBLANK VBL
         BLNK_WFM CBLANK
SETF /CLK /XH /EV /OD /R /S0 /S1 /S2 /C0 /C1 /HBLANK /VBL /CLAMP
FOR X := 1 TO 10 DO
BEGIN
SETF CLK
SETF /CLK
END

SETF XH                    ;red text on xhatch background
SETF /XH
SETF CLK
SETF /CLK
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END
SETF EV
SETF OD
SETF R
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END
SETF /EV
SETF /OD
SETF /R
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END

SETF S2 /S1 S0             ;red text on grayscale backgound
SETF R
SETF /R
SETF CLK
SETF /CLK
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END
SETF EV
SETF OD
SETF R
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END
SETF /EV
SETF /OD
SETF /R
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
```

```
END

SETF S2 S1 /S0              ;external video
SETF /R
SETF R
SETF /R
SETF CLK
SETF /CLK
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END
SETF EV
SETF OD
SETF R
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END
SETF /EV
SETF /OD
SETF /R
FOR X := 1 TO 5 DO
BEGIN
SETF CLK
SETF /CLK
END

SETF HBL
SETF CLAMP
SETF /CLAMP
SETF /HBL
SETF VBL
SETF HBL
SETF CLAMP
SETF /CLAMP
SETF /HBL
SETF /VBL

TRACE_OFF

;-------------------------------------------------------------------------
```

```
;PALASM Design Description

;------------------------ Declaration Segment ------------------------------

TITLE     TEXT20 - Character Generator Timing Controller
PATTERN   U111 of Control Board
REVISION  2.0
AUTHOR    Joel Tarback, A. Koebel
COMPANY   ELECTROHOME LTD.
DATE      March 6, 1993

CHIP  TEXT   MACH110

;------------------------ Description -------------------------------------
;
; This IC provides many of the timing signals required to scan characters
; out to the display. It contains an up-counter clocked by PIXCLKB that
; divides the active horizontal scan time into 64 time slots (columns). It
; also contains a vertical counter clocked by VLTC, from the vertical RAM
; circuit (U102 etc.), that divides the raster into 24 rows. In addition,
; it outputs signals which are used to generate a grayscale test pattern.
;
; Text is displayed on-screen in a 64 column by 24 row matrix. A 16-bit word
; is stored for each screen location in RAMs U97 and U98. During the first
; half of each horizontal time slot, U111 generates a column address
; (CG0-CG5) and a row address (CG6-CG11) for the RAMs to specify one of the
; screen locations. It also drives CG12 low to address the lower half of the
; RAM space. The RAMs then each output a byte. These are loaded into latches
; U89 and U91 using FONT_CLK (FONT-CLK).
;
; During the second half of the horizontal time slot, the data in U91 is fed
; back to the RAMs on CG4-CG11. CG12 is driven low to address the upper half
; of the RAM space. This address selects one of the character bitmaps.
; OEFONT (OEFONT*) is driven low to mux address data from the vertical RAM
; circuit onto CG0-CG3, selecting which line of pixels in the bitmap will be
; displayed on the current scan line. In response to the combined address on
; CG0-CG12, the RAMs each output another byte. These are loaded into shift
; registers U88 and U99 using LDSHIFT (LOADSHIFT*). The pixels in these
; registers are shifted out for display during the next horizontal time slot.
;
; The three most significant bits of the horizontal count are output as GR0,
; GR1, and GR2 (HCOUNT5*, HCOUNT6*, and HCOUNT7*). These are used to create
; the grayscale test pattern. MIDV from the vertical RAM circuit inverts
; these outputs midway down the raster.
;
; Revision History:
;
;   1.X - all 1.X versions were based on a pin-compatible MACH 210 device
;         and implemented variable width characters (8,12 or 16 pixels).
;   2.0 - first version for MACH 110, with fixed width characters (8 pixels)
;
;------------------------ PIN Declarations --------------------------------

;CLOCKS AND INPUTS:

PIN   35   PIXCLKB   COMBINATORIAL ; INPUT   pixel clock (buffered)
PIN   13   HEN2      COMBINATORIAL ; INPUT   from pin 4 (HEN1) and used as clock
PIN   10   OE244     COMBINATORIAL ; INPUT   enable for row and column addresses
PIN   11   VDRIVE    COMBINATORIAL ; INPUT   video field reset for row counter
PIN   32   OE        COMBINATORIAL ; INPUT   global tristate for all outputs
PIN   33   HCLK      COMBINATORIAL ; INPUT   same as PIXCLKB but combinatorial
```

```
;SEGMENT A:

PIN   2   HC3       COMBINATORIAL ; OUTPUT counter output - dense xhatch lines
PIN   4   HEN1         REGISTERED ; OUTPUT active video enable
PIN   5   HX        COMBINATORIAL ; OUTPUT vertical xhatch lines
PIN   6   START_HB  COMBINATORIAL ; INPUT  start of horizontal count
PIN   7   VLTC      COMBINATORIAL ; INPUT  clock for row counter
NODE  3   HTC          REGISTERED ; OUTPUT
PIN   14  GR0          REGISTERED ; OUTPUT grayscale - LSb
PIN   15  GR1          REGISTERED ; OUTPUT grayscale
PIN   16  GR2          REGISTERED ; OUTPUT grayscale - MSb
PIN   17  MIDV      COMBINATORIAL ; INPUT  lower half of raster (for grayscale)
PIN   18  FONT_CLK     REGISTERED ; OUTPUT clocks and muxes font address/data
PIN   19  LDSHIFT      REGISTERED ; OUTPUT loads output shift registers
PIN   20  OEFONT    COMBINATORIAL ; OUTPUT muxes font and font slices
PIN   21  CG12      COMBINATORIAL ; OUTPUT selects font or character from RAM
NODE  13  ELS          REGISTERED ; OUTPUT
NODE  9   OEROW     COMBINATORIAL ; OUTPUT muxes row and column addresses

GROUP MACH_SEG_A HEN1 HTC FONT_CLK LDSHIFT ELS GR0 GR1 GR2

;SEGMENT B:

PIN   24  COL0          REGISTERED ; OUTPUT column count   - CG0
PIN   25  COL1          REGISTERED ; OUTPUT column count   - CG1
PIN   26  COL2          REGISTERED ; OUTPUT column count   - CG2
PIN   27  COL3          REGISTERED ; OUTPUT column count   - CG3
PIN   28  COL4          REGISTERED ; OUTPUT column count   - CG4
PIN   29  COL5          REGISTERED ; OUTPUT column count   - CG5
NODE  33  COL6          REGISTERED ; OUTPUT column count
PIN   36  ROW0          REGISTERED ; OUTPUT row count      - CG6
PIN   37  ROW1          REGISTERED ; OUTPUT row count      - CG7
PIN   38  ROW2          REGISTERED ; OUTPUT row count      - CG8
PIN   39  ROW3          REGISTERED ; OUTPUT row count      - CG9
PIN   40  ROW4          REGISTERED ; OUTPUT row count      - CG10
PIN   41  ROW5       COMBINATORIAL ; OUTPUT dummy row bit  - CG11
PIN   42  ATC           REGISTERED ; OUTPUT same as ROW0 but not tristated

GROUP MACH_SEG_B CG0 COL1 COL2 COL3 COL4 COL5 COL6

;------------------------- Boolean Equation Segment -------------------------

EQUATIONS

;SEGMENT A:

HTC=COL6*/LDSHIFT
HEN1.T=HEN1*START_HB+/HEN1*HTC
HC3=COL1

MACH_SEG_A.CLKF=PIXCLKB
MACH_SEG_A.SETF=GND
MACH_SEG_A.RSTF=GND

HX=ELS*/FONT_CLK*/HCLK*COL0        ;Vertical crosshatch lines
HC3.TRST=OE
HEN1.TRST=OE                       ;Global tristates
HX.TRST=OE

GR2.T=/LDSHIFT*(MIDV*/COL5*/GR2    ;Grayscale outputs
              +MIDV*COL5*GR2
              +/MIDV*/COL5*GR2
              +/MIDV*COL5*/GR2)
```

```
GR1.T=/LDSHIFT*(MIDV*/COL4*/GR1
              +MIDV*COL4*GR1
              +/MIDV*/COL4*GR1
              +/MIDV*COL4*/GR1)
GR0.T=/LDSHIFT*(MIDV*/COL3*/GR0
              +MIDV*COL3*GR0
              +/MIDV*/COL3*GR0
              +/MIDV*COL3*/GR0)

FONT_CLK.T=/FONT_CLK*/HEN1*/ELS +FONT_CLK*(HEN1+/LDSHIFT)
LDSHIFT.T=LDSHIFT*/HEN1*FONT_CLK  +/LDSHIFT
ELS=FONT_CLK

OEFONT=/OE244+/FONT_CLK+HEN1
GR0.TRST=OE
GR1.TRST=OE
GR2.TRST=OE
FONT_CLK.TRST=OE                  ;Global tristates
LDSHIFT.TRST=OE
OEFONT.TRST=OE


;SEGMENT B:

COL6.T=/LDSHIFT*/HEN1*COL0*COL1*COL2*COL3*COL4*COL5 +HEN1*COL6
COL5.T=/LDSHIFT*/HEN1*COL0*COL1*COL2*COL3*COL4      +HEN1*COL5
COL4.T=/LDSHIFT*/HEN1*COL0*COL1*COL2*COL3           +HEN1*COL4
COL3.T=/LDSHIFT*/HEN1*COL0*COL1*COL2                +HEN1*COL3
COL2.T=/LDSHIFT*/HEN1*COL0*COL1                     +HEN1*COL2
COL1.T=/LDSHIFT*/HEN1*COL0                          +HEN1*COL1
COL0.T=/LDSHIFT*/HEN1                               +HEN1*COL0
COL5.TRST=OEROW*OE                ;Column counters
COL4.TRST=OEROW*OE                ;Muxed by OEROW
COL3.TRST=OEROW*OE                ;Globally tristated
COL2.TRST=OEROW*OE
COL1.TRST=OEROW*OE
COL0.TRST=OEROW*OE

ROW5=GND                                                ;Dummy row count
ROW4.T=/VDRIVE*VXLIN*ROW0*ROW1*ROW2*ROW3 +VDRIVE*ROW4   ;ROW0-ROW4 = row count
ROW3.T=/VDRIVE*VXLIN*ROW0*ROW1*ROW2      +VDRIVE*ROW3
ROW2.T=/VDRIVE*VXLIN*ROW0*ROW1           +VDRIVE*ROW2
ROW1.T=/VDRIVE*VXLIN*ROW0                +VDRIVE*ROW1
ROW0.T=/VDRIVE*VXLIN                     +VDRIVE*ROW0
ATC.T=/VDRIVE*VXLIN                      +VDRIVE*ROW0
ROW5.TRST=OEROW*OE
ROW4.TRST=OEROW*OE
ROW3.TRST=OEROW*OE
ROW2.TRST=OEROW*OE                ;Muxed by OEROW
ROW1.TRST=OEROW*OE                ;Globally tristated
ROW0.TRST=OEROW*OE
ATC.TRST=OE

CG12=FONT_CLK                     ;Selects half or RAM, character or font
CG12.TRST=OE244*OE

OEROW=OE244*/FONT_CLK*/HEN1       ;Row and column output enable or mux

ROW0.CLKF=HEN2
ROW0.SETF=GND
ROW0.RSTF=GND
ROW1.CLKF=HEN2
ROW1.SETF=GND
ROW1.RSTF=GND
```

```
ROW2.CLKF=HEN2
ROW2.SETF=GND
ROW2.RSTF=GND
ROW3.CLKF=HEN2
ROW3.SETF=GND
ROW3.RSTF=GND
ROW4.CLKF=HEN2
ROW4.SETF=GND
ROW4.RSTF=GND
ATC.CLKF=HEN2
ATC.SETF=GND
ATC.RSTF=GND

MACH_SEG_B.CLKF=PIXCLKB
MACH_SEG_B.SETF=GND
MACH_SEG_B.RSTF=GND


;------------------------- Simulation Segment ----------------------------
SIMULATION

TRACE_ON PIXCLKB OE244 HEN1 HEN2 START_HB H3 HX OE MIDV GR0 GR1 GR2
         FONT_CLK LDSHIFT ELS OEFONT CG12 COL0 COL1 COL2 COL3 COL4 COL5
         COL6 HTC OEROW ATC ROW0 ROW1 ROW2 ROW3 ROW4 ROW5 VDRIVE VXLIN

SETF /PIXCLKB OE244 /START_HB /MIDV /VDRIVE HEN2 /VXLIN OE /HC3

PRELOAD HEN1

FOR X := 1 TO 5 DO
BEGIN
SETF PIXCLKB HC3
SETF /PIXCLKB /HC3
END

SETF START_HB

SETF PIXCLKB HC3 /HEN2

SETF /PIXCLKB /HC3

SETF /START_HB

FOR X := 1 TO 259 DO
BEGIN
SETF PIXCLKB HC3
SETF /PIXCLKB /HC3
END

SETF HEN2

FOR X := 1 TO 11 DO
BEGIN
SETF PIXCLKB HC3
SETF /PIXCLKB /HC3
END

TRACE_OFF

;-------------------------------------------------------------------------
```

```
;PALASM Design Description

;--------------------------- Declaration Segment ---------------------

TITLE     XHATCH11 - Crosshatch Generator
PATTERN   U117 of Control Board
REVISION  1.1
AUTHOR    J.Tarback, A. Koebel
COMPANY   ELECTROHOME LTD.
DATE      12/14/92

CHIP  XHATCH  PALCE16V8

;---------------------------- Description -----------------------------
;
; This PAL, with the aid of delay line U109, creates four types of
; test patterns; standard crosshatch, dense crosshatch, dot field
; and crosshatch with dots. Horizontal crosshatch lines are created
; using ATC from PLD U111 and VLTC from the vertical RAM circuit (U102
; etc). Vertical lines are created using HX and HC3 from U111. The HX
; signal is composed of 32 narrow pulses on every scan line. Each pulse
; has a width of one half cycle of clock signal PIXCLKB from the DPB.
; HX is input to the delay line, which outputs delayed versions TAP1 to
; TAP7, each delayed by a multiple of 5 nsec. These are input to the
; PAL, which selects one of the signals according to the code 'K'
; formed by W0-W2 from register U94. The delayed pulses are ORed with
; the first tap. This narrows the width of the pulses, resulting in
; thinner vertical crosshatch lines. The width is chosen by software
; according to the horizontal scan frequency.
;
; The horizontal and vertical lines are ANDed to create a crosshatch
; and ORed to create dots. S0 (SELECT0) and S1 (SELECT1) from
; register U94 select one of the four possible test patterns for output
; on XHATCH. This output is mixed with text pixels in PAL U108.
;
; Revision History:
;
;   V1.0 - original
;   V1.1 - changed code K=1 to give 0 ns delay instead of 5 ns to
;          make brighter vertical lines for 80 kHz - 100 kHz
;
;--------------------------- PIN Declarations --------------------------

PIN   1  TAP1     COMBINATORIAL ; INPUT  delay line output - 5 ns
PIN   2  TAP2     COMBINATORIAL ; INPUT  delay line output - 10 ns
PIN   3  TAP3     COMBINATORIAL ; INPUT  delay line output - 15 ns
PIN   4  TAP4     COMBINATORIAL ; INPUT  delay line output - 20 ns
PIN   5  TAP5     COMBINATORIAL ; INPUT  delay line output - 25 ns
PIN   6  TAP6     COMBINATORIAL ; INPUT  delay line output - 30 ns
PIN   7  TAP7     COMBINATORIAL ; INPUT  delay line output - 35 ns
PIN   8  W2       COMBINATORIAL ; INPUT
PIN   9  W0       COMBINATORIAL ; INPUT  W0-W2 = code for selection
PIN   10 GND                                     of delay line tap
PIN   11 W1       COMBINATORIAL ; INPUT
PIN   12 IO0                    ; OUTPUT not connected
PIN   13 LINE     COMBINATORIAL ; OUTPUT partial logic, not connected
PIN   14 HC3      COMBINATORIAL ; INPUT  horizontal count from U111
PIN   15 ATC      COMBINATORIAL ; INPUT  vertical count from U111
PIN   16 VLTC     COMBINATORIAL ; INPUT  vertical clock (horiz. lines)
PIN   17 S1       COMBINATORIAL ; INPUT  S0,S1 = code for selection
PIN   18 S0       COMBINATORIAL ; INPUT          of test pattern
PIN   19 XHATCH   COMBINATORIAL ; OUTPUT test pattern output to U108
PIN   20 VCC
```

```
;-------------------------- Boolean Equation Segment -----------------

EQUATIONS
;                                          K   Width Reduction
;                                         ---  ---------------
LINE = /W0 * /W1 * /W2 * TAP1             ;0 -  0 ns narrower
     +  W0 * /W1 * /W2 * TAP1             ;1 -  0 ns narrower  (was 5 ns)
     + /W0 * W1 * /W2 * TAP1 * TAP3       ;2 - 10 ns narrower
     + W0 * W1 * /W2 * TAP1 * TAP4        ;3 - 15 ns narrower
     + /W0 * /W1 * W2 * TAP1 * TAP5       ;4 - 20 ns narrower
     + W0 * /W1 * W2 * TAP1 * TAP6        ;5 - 25 ns narrower
     + /W0 * W1 * W2 * TAP1 * TAP7        ;6 - 30 ns narrower

XHATCH = /S0 * /S1 * (VLTC + LINE)                                ;dense xhatch
       + S0 * /S1 * (VLTC * /ATC + LINE * HC3)                    ;normal xhatch
       + /S0 * S1 * (VLTC * LINE)                                 ;dots
       + S0 * S1 * (VLTC * /ATC + LINE * HC3 + VLTC * LINE)       ;dots & xhatch

;-------------------------- Simulation Segment ----------------------

SIMULATION

;Does not simulate totally, just a very small crosshatch

TRACE_ON TAP1 TAP2 W0 W1 W2 LINE HC3 VLTC ATC S0 S1 XHATCH

SETF TAP1 TAP2 /TAP3 /TAP4 /TAP5 /TAP6 /TAP7 W0 W1 W2 /S0 /S1
SETF /HC3 /VLTC /ATC /W0 /W1 /W2

FOR Y := 1 TO 3 DO
BEGIN
FOR X := 1 TO 3 DO
BEGIN
SETF /TAP1 /TAP2
END
SETF HC3
SETF TAP1 TAP2
SETF /HC3
FOR X := 1 TO 3 DO
BEGIN
SETF /TAP1 /TAP2
END
SETF TAP1 TAP2
END

SETF S0 /S1
FOR Y := 1 TO 3 DO
BEGIN
FOR X := 1 TO 3 DO
BEGIN
SETF /TAP1 /TAP2
END
SETF HC3
SETF TAP1 TAP2
SETF /HC3
FOR X := 1 TO 3 DO
BEGIN
SETF /TAP1 /TAP2
END
SETF TAP1 TAP2
END
```